


**Quanta Project Name: XM1**

**Dell Project Name: Nike**

**2008-03-18**

**REV : A1A**

**X01 Stage**

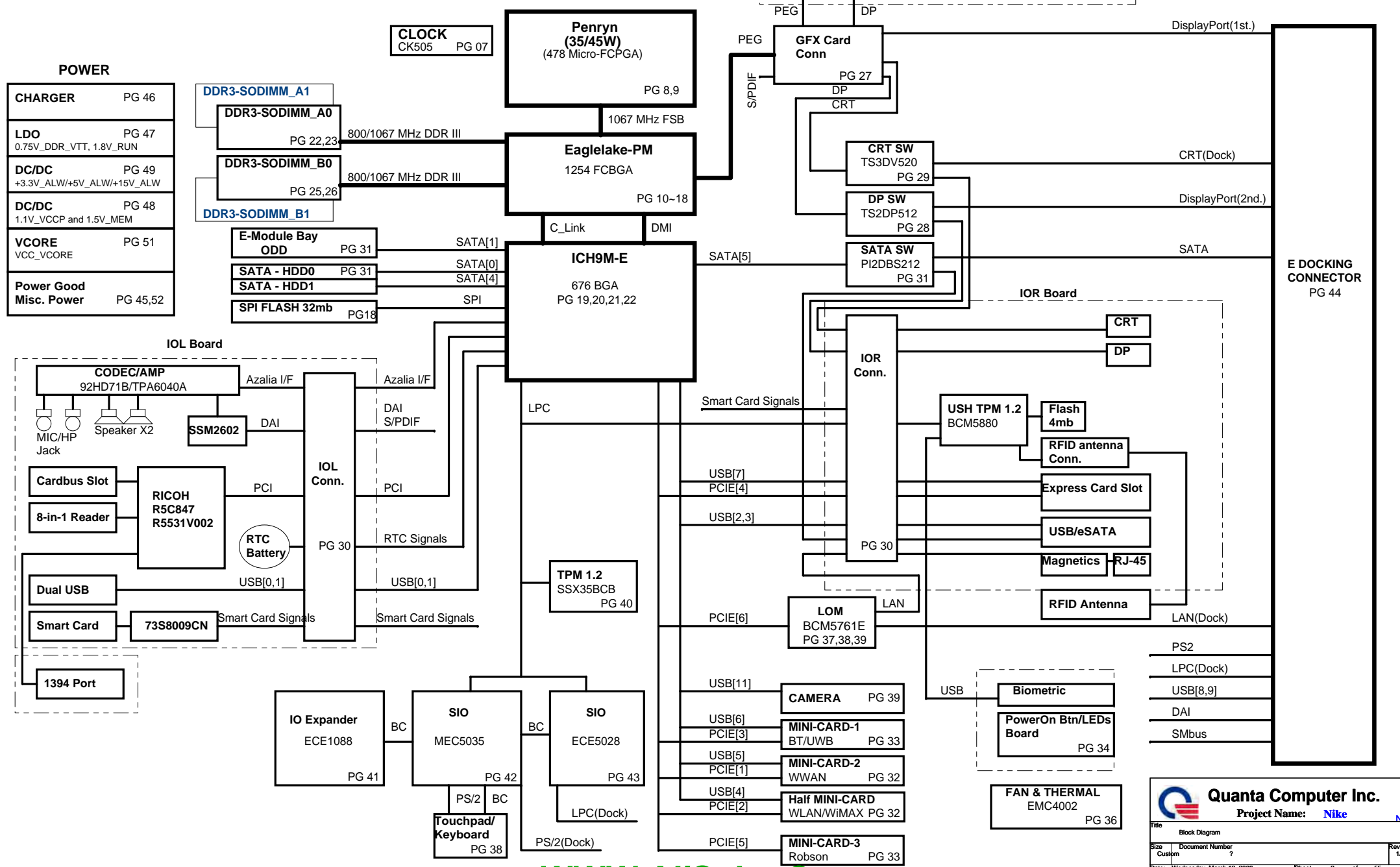
		<b>Quanta Computer Inc.</b>	
		Project Name: <b>Nike</b> NB1	
Title Cover Page			
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XM1 M/B PCB

# System Block Diagram of Nike

PWA XXX, PWB XXX,  
SCHEM XXX.  
VER : XX Date: 071010




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35	CCD SNIFFER LED.
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41	IO EXPAND_ECE1088
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43	SIO-ECE5028
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47	0.75V_DDR_VTT, 1.8V_RUN
48	1.1V_VCCP and 1.5V_MEM
49	5V_ALW, 3V_ALW
50	DCIN, Battery Connector
51	CPU_VCORE (ADP3207A)
52	Power Misc
53	Screw hole

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

Power Plane State	+15V_ALW +5V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.75V_DDR_VTT +1.1V_VCCP +VCC_CORE
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

ICH9M-E	USB PORT#	DESTINATION
	0	Left Top
	1	Left Bot
	2	Right Top
	3	Right Bot
	4	WLAN
	5	WWAN
	6	WPAN
	7	Express card
	8	DOCKING
	9	DOCKING
	10	USH
	11	Camera

ICH9M-E	PCI EXPRESS	DESTINATION
	Lane 1	WWAN
	Lane 2	WLAN
	Lane 3	BT/UWB
	Lane 4	Express Card
	Lane 5	Robson
	Lane 6	Giga Bit LOM



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File

Index and Config.

Size

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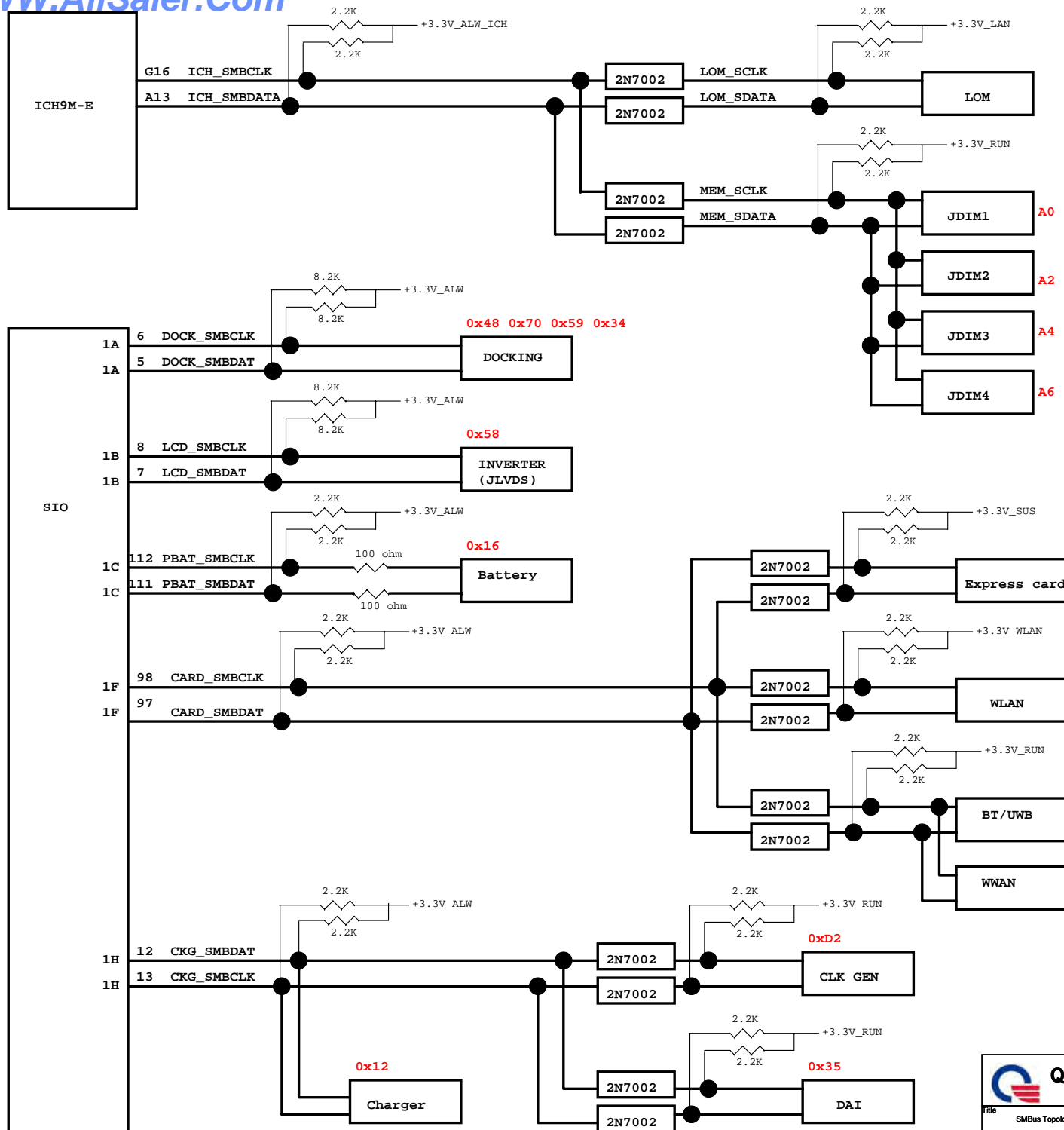
Custom

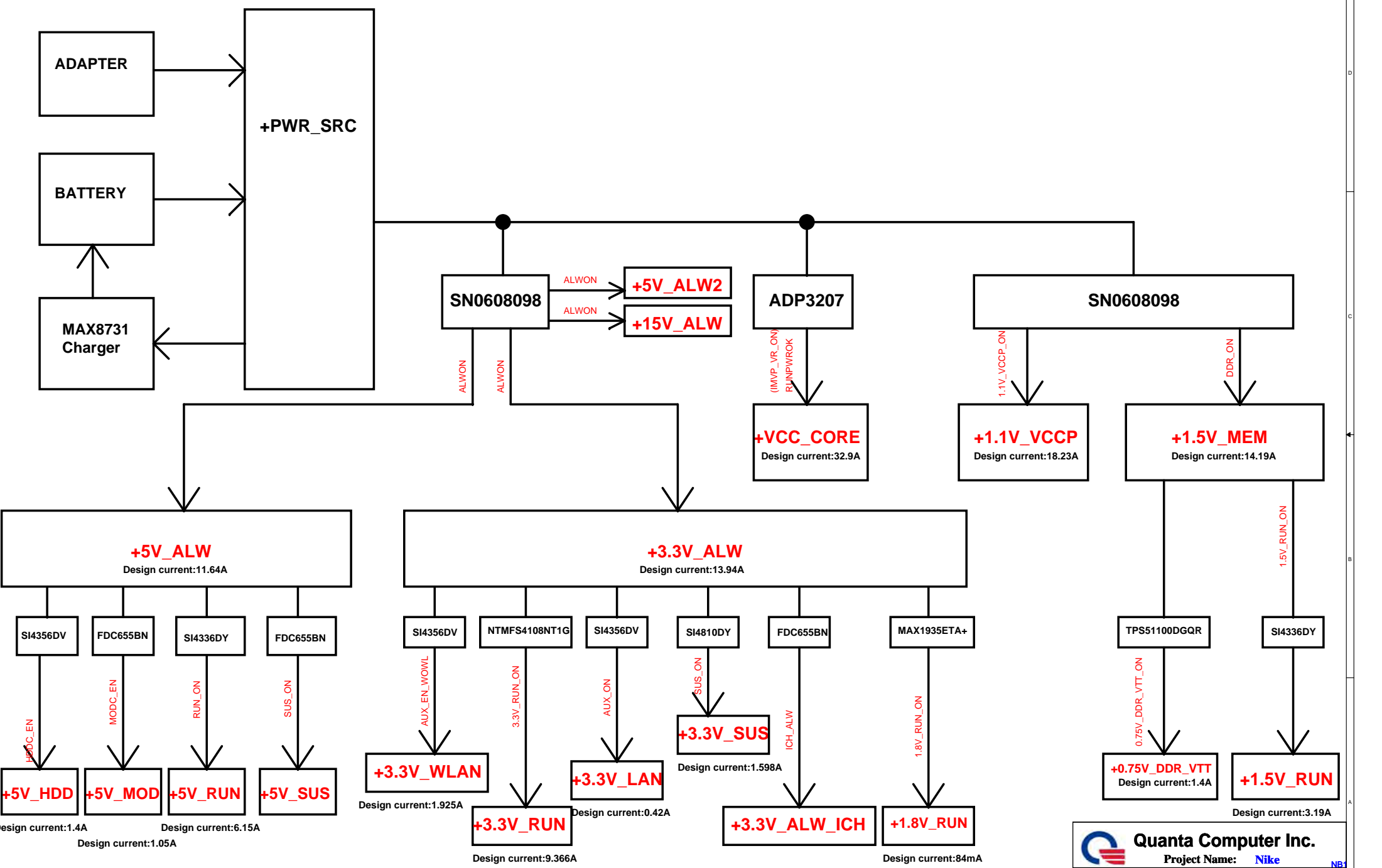
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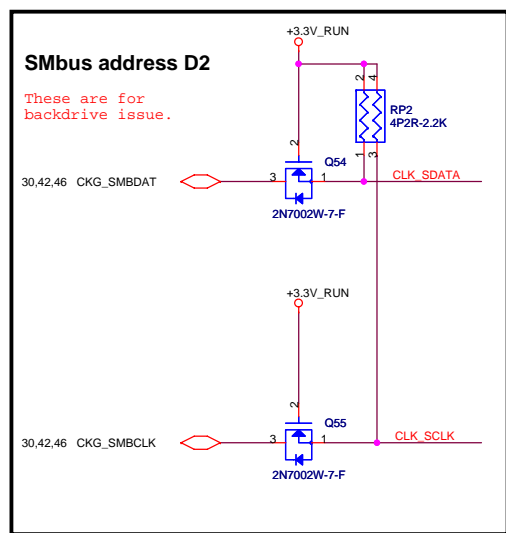
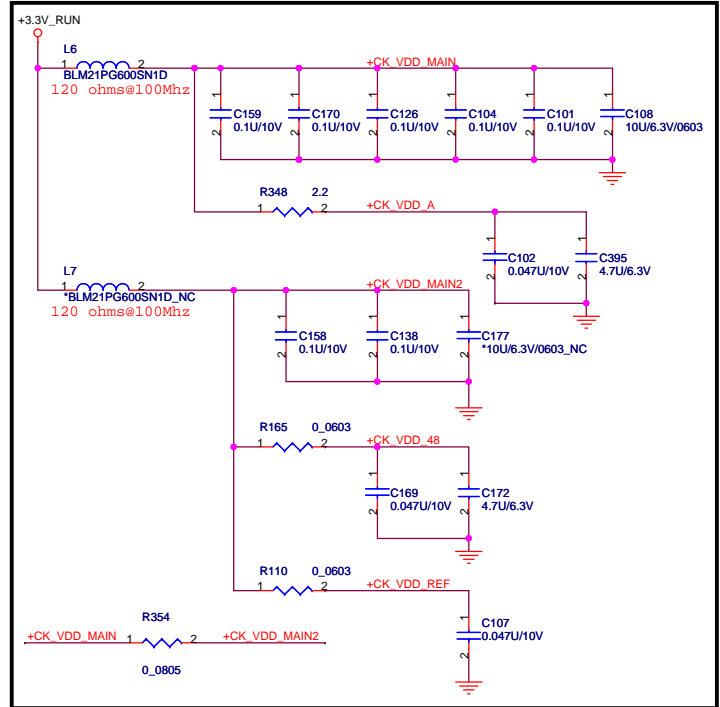
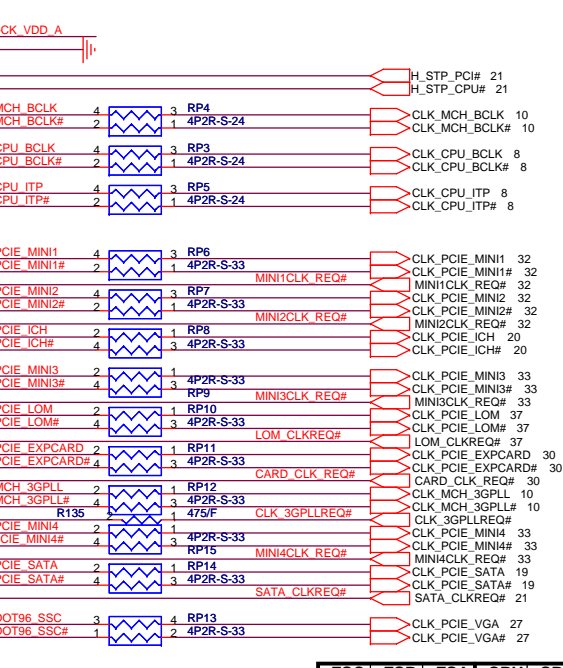
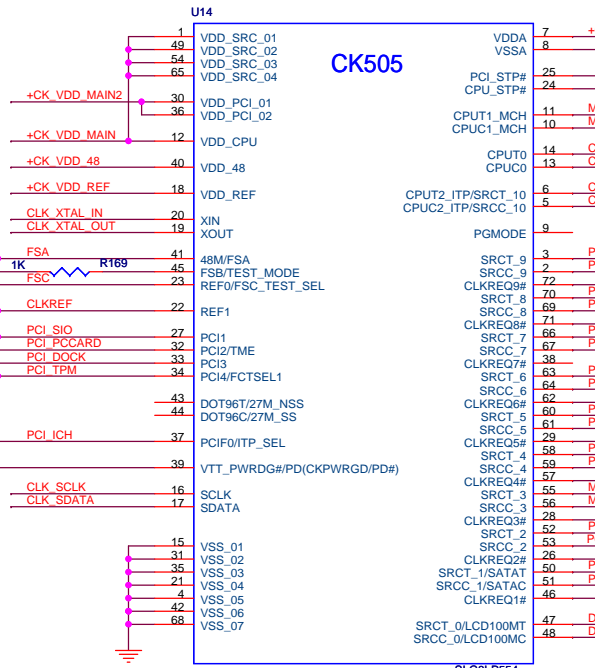
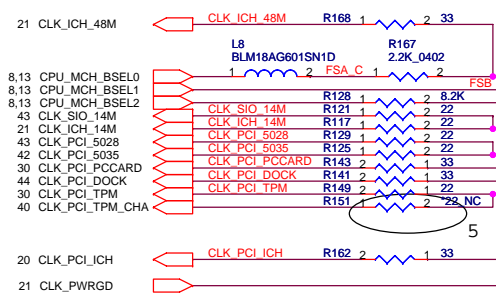
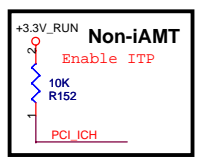
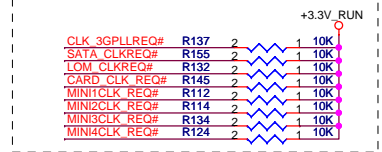
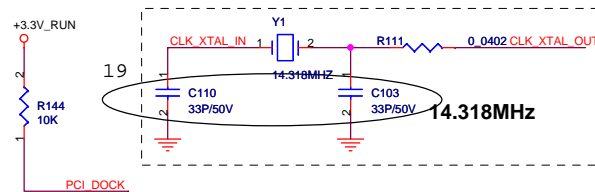
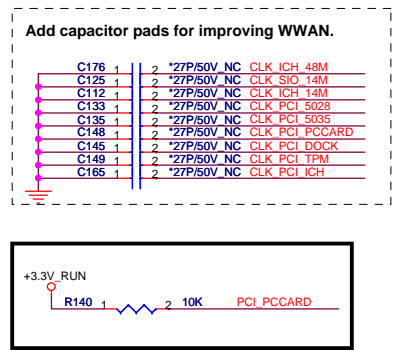
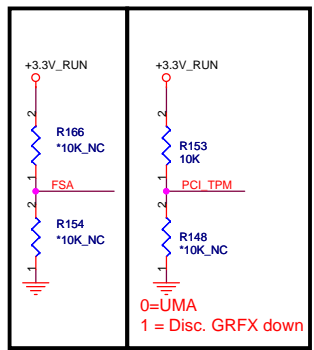


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Project Name: Nike

NB3

Title		Screw hole	
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FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	RSVD	RSVD

PCI\_LOM = FCTSEL1

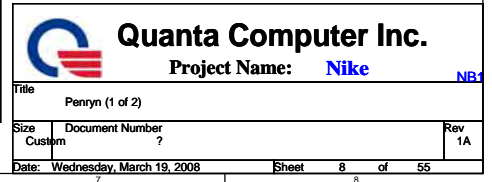
FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0

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Project Name: Nike

Title: Clock Generator

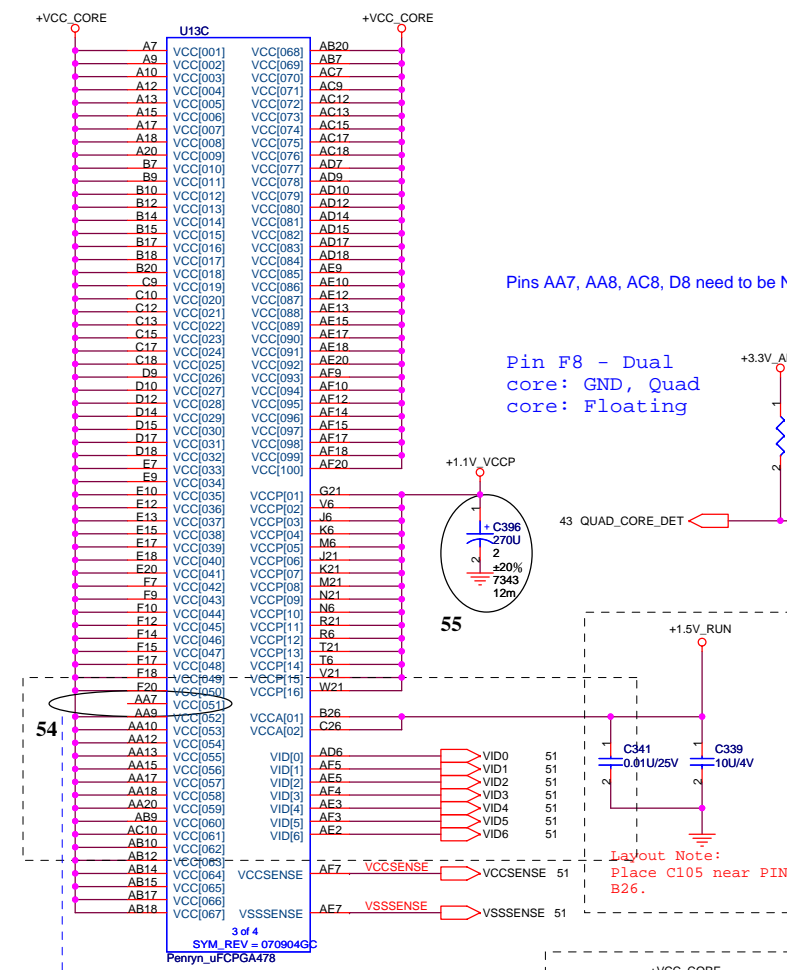
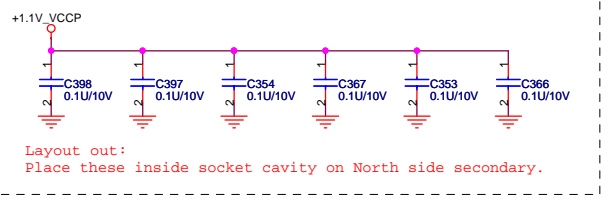
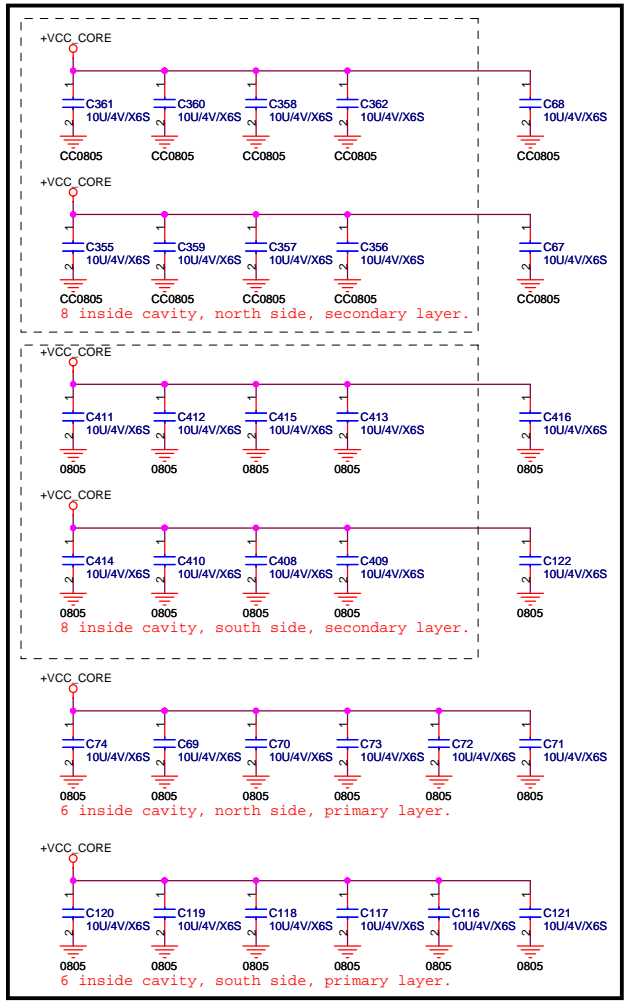
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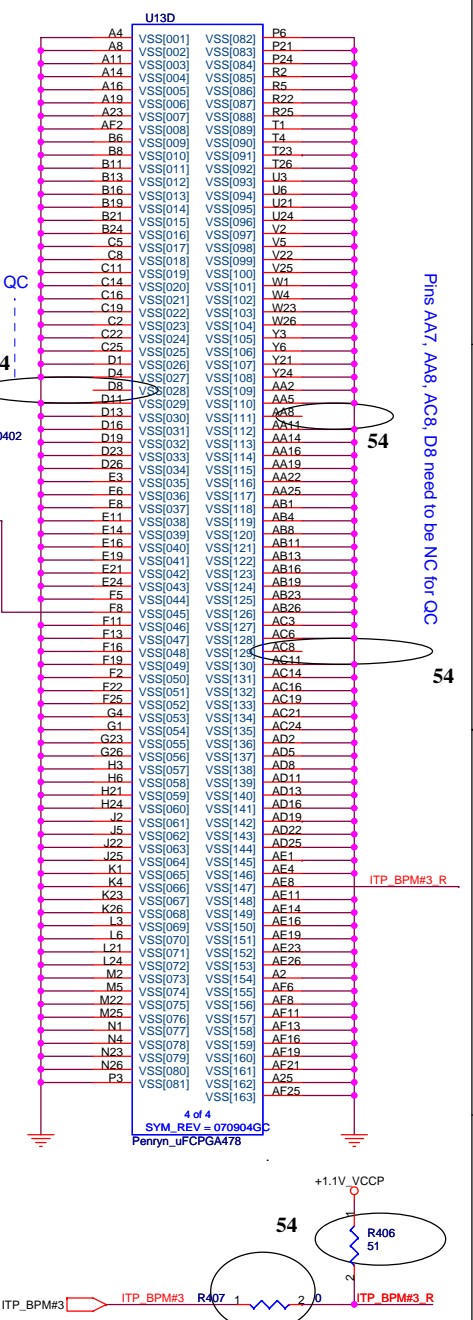
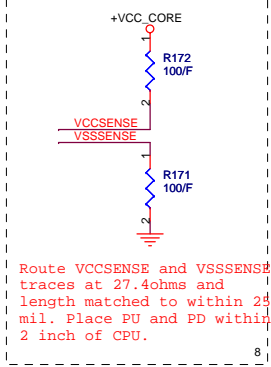




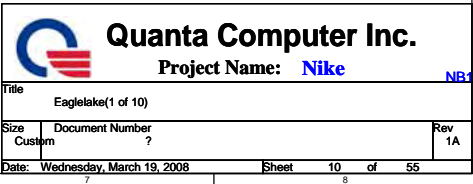
All use 220 10V(+20%,X5R,1210)Pb-Free.

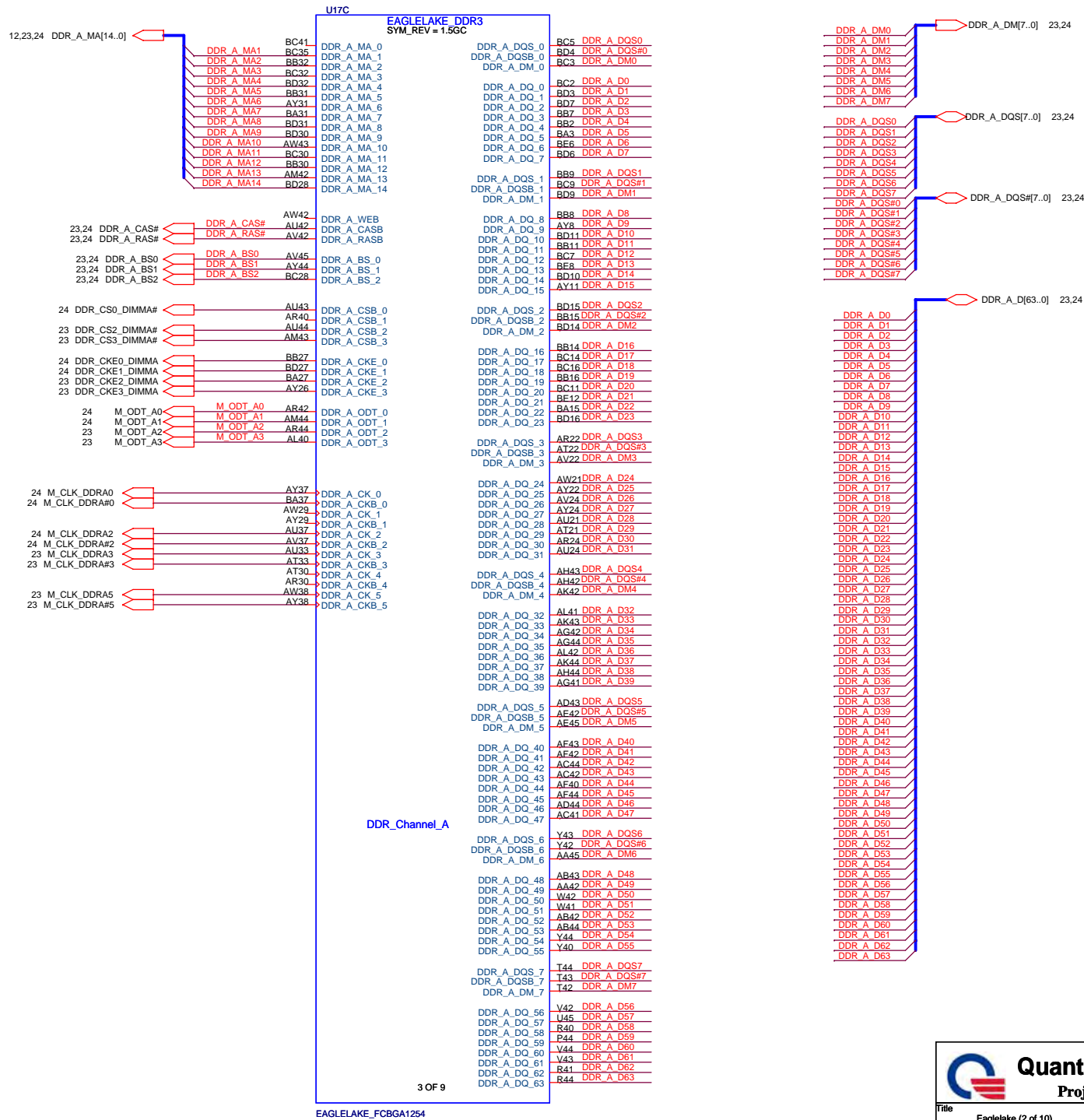


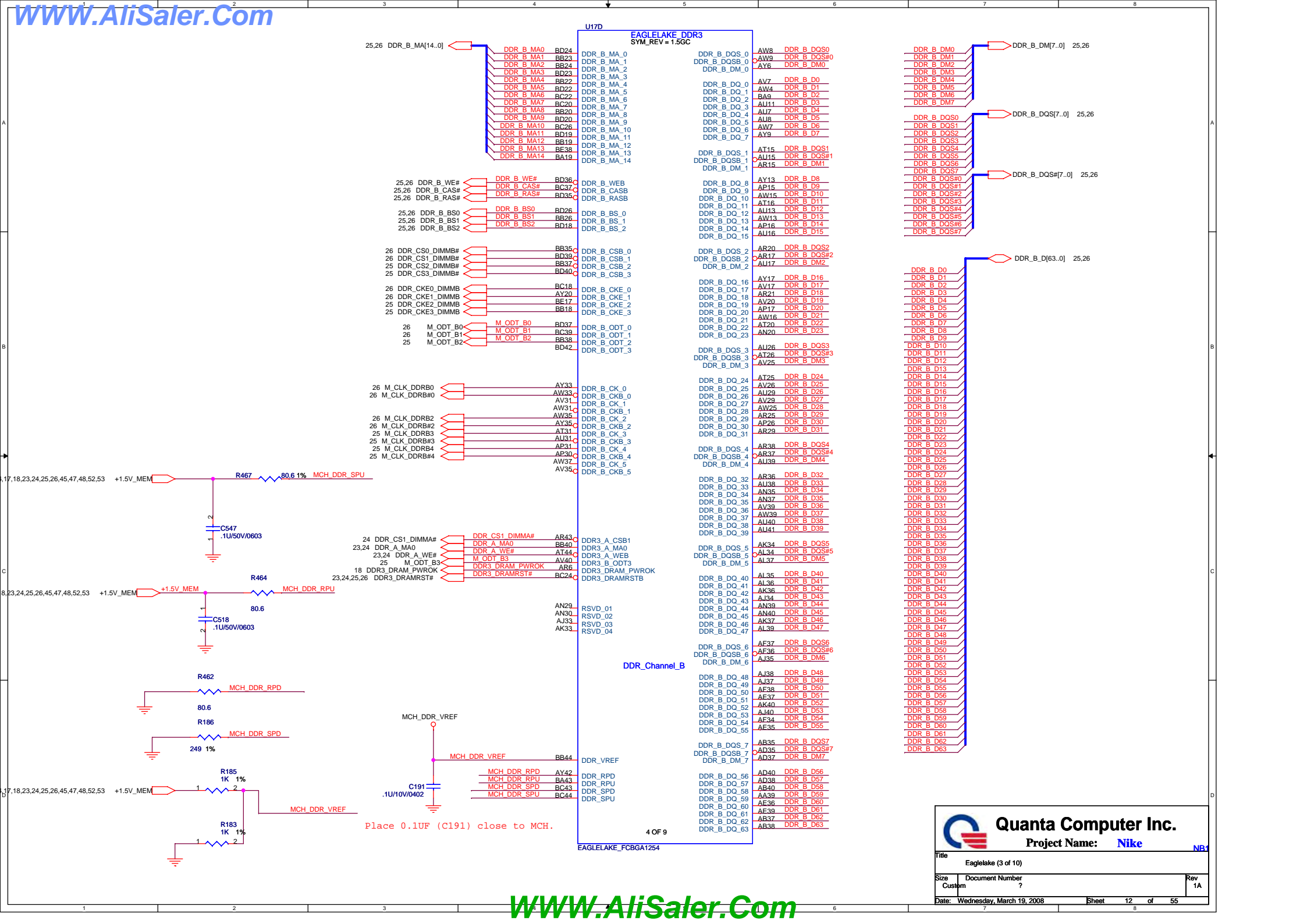
Pins AA7, AA8, AC8, D8 need to be NC for QC




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Project Name: <b>Nike</b>		NB1	
Title	Penryn (2 of 2)		
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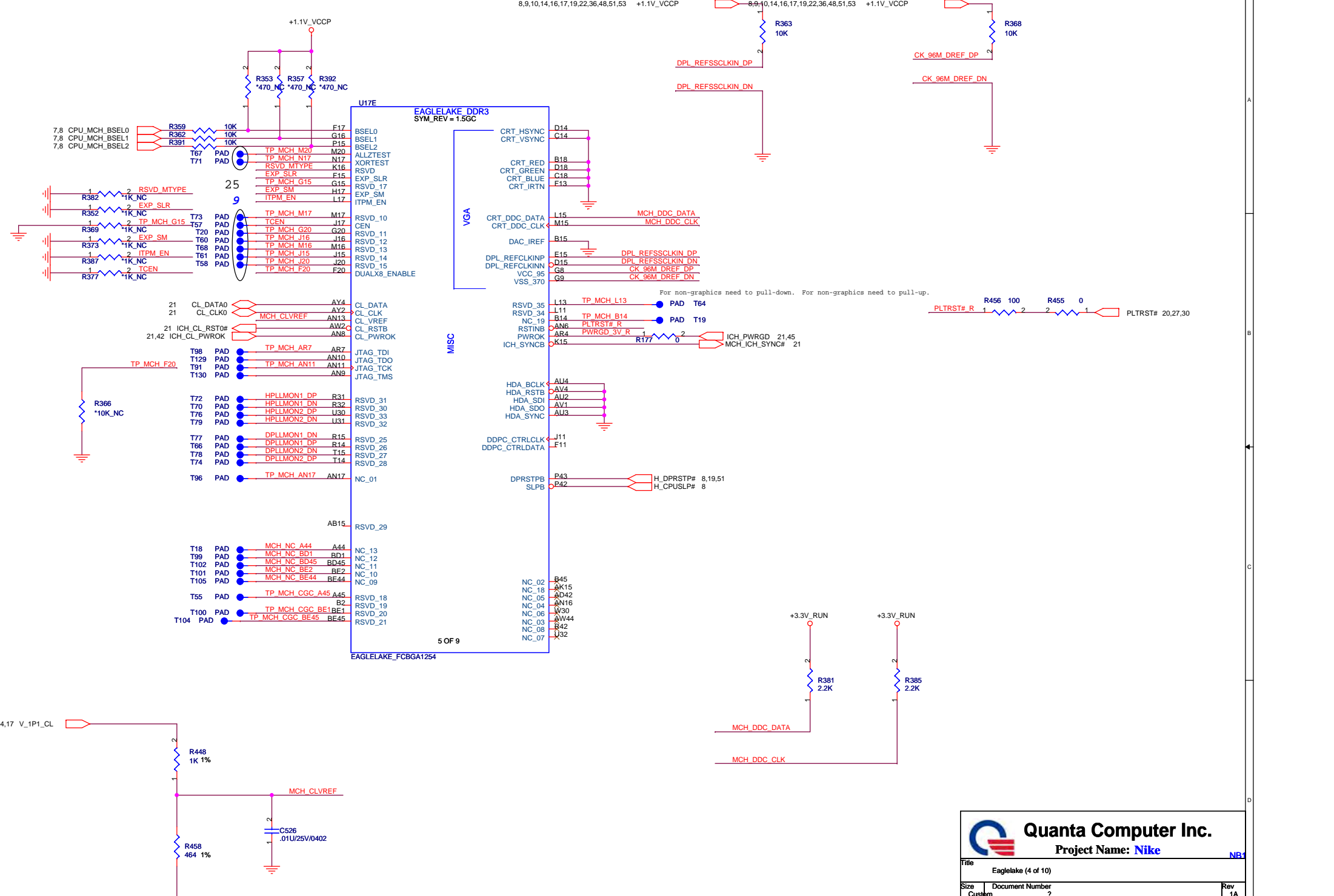
Quanta Computer Inc.


Project Name: Nike

TitleEaglelake (3 of 10)

SizeCustomDocument Number ?Rev1A

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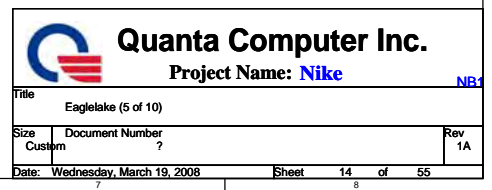


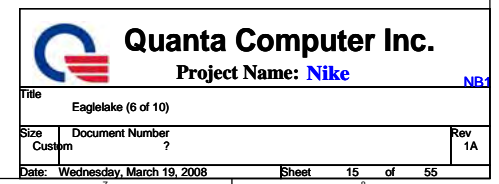
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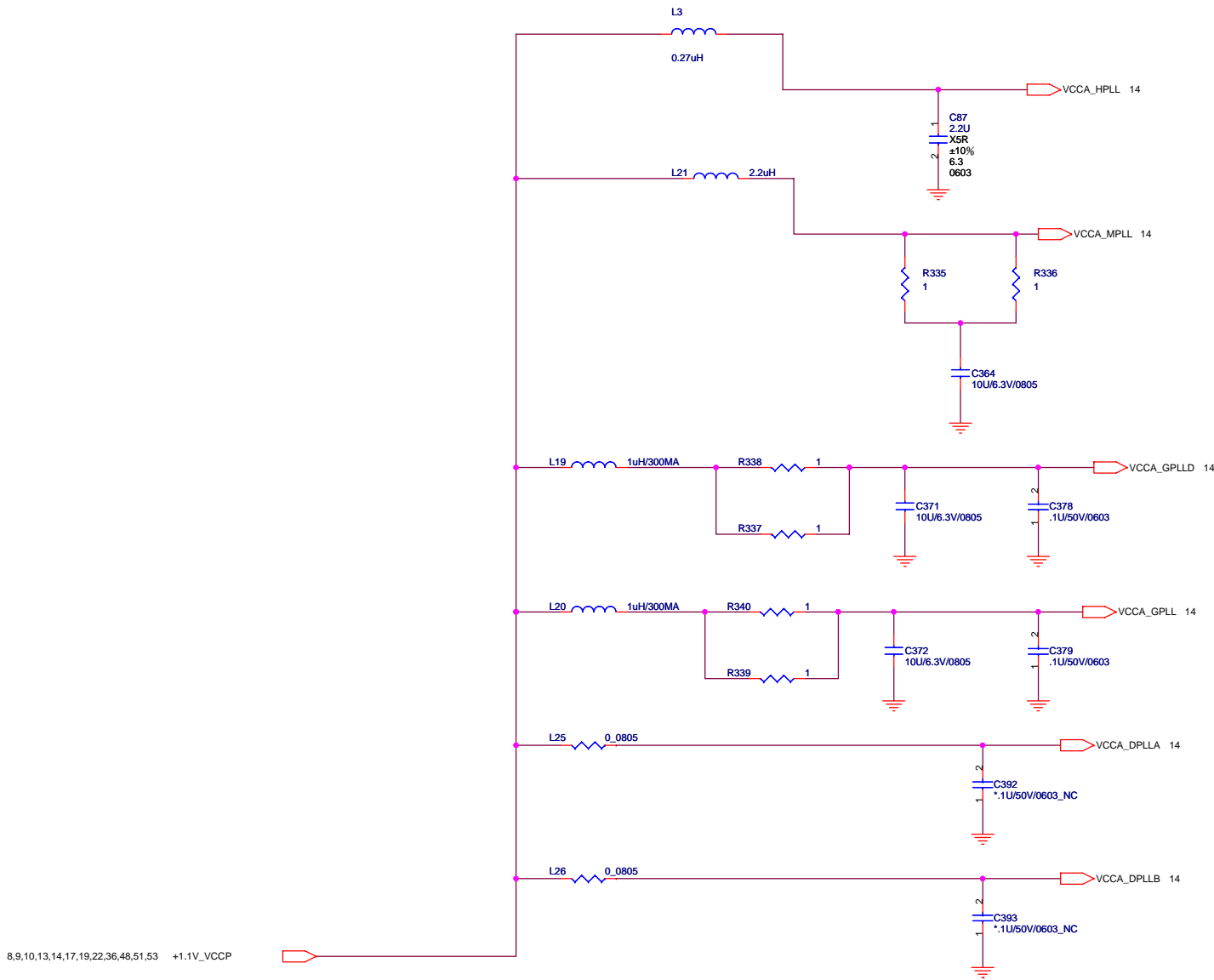
Project Name: Nike


Title		Eaglelake (4 of 10)	
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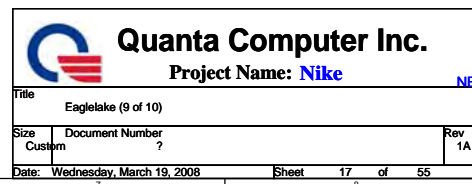


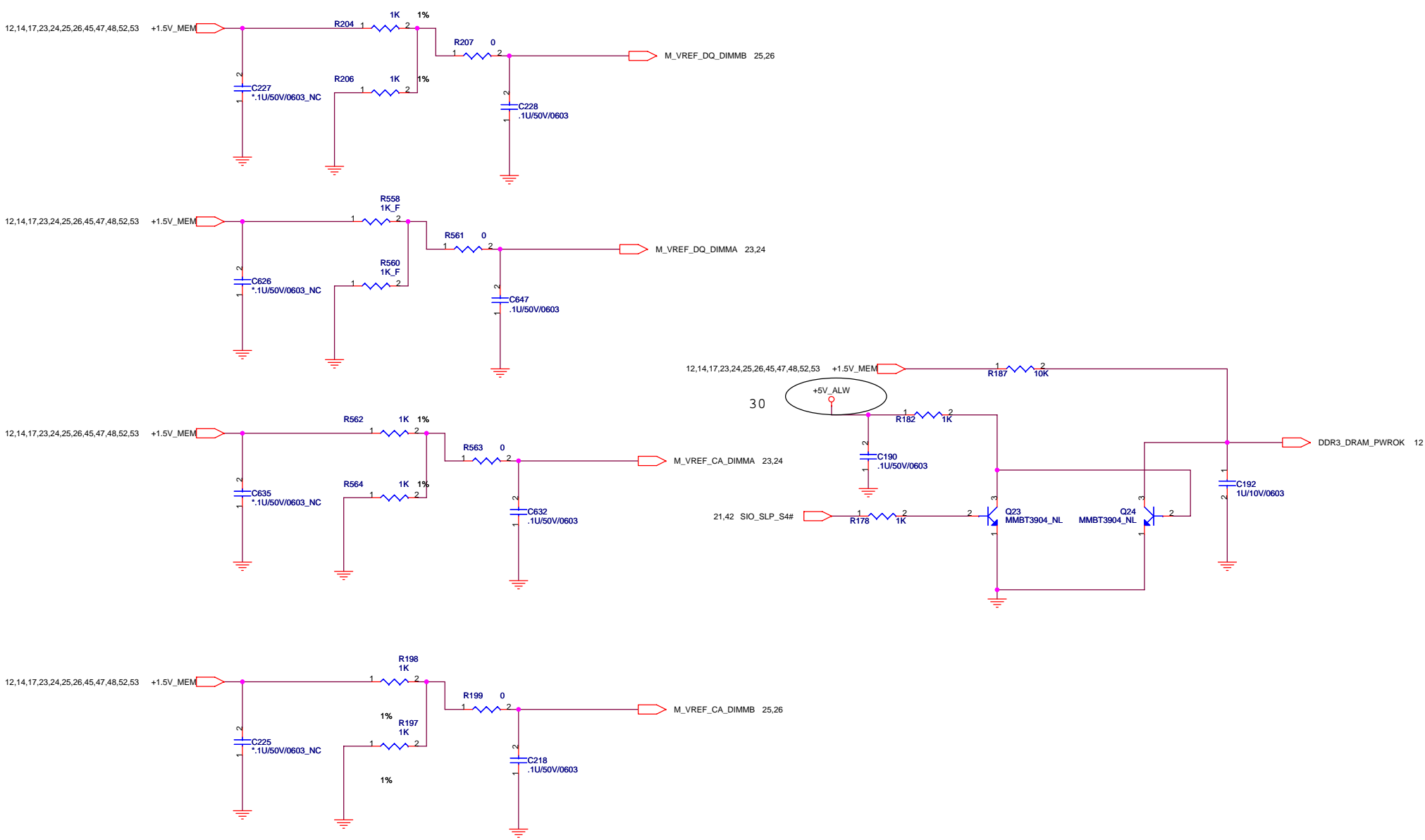
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Project Name: Nike

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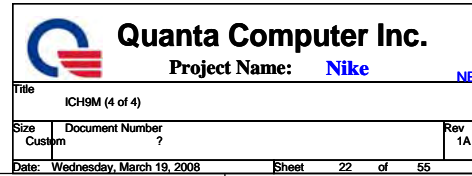
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Project Name: **Nike**

Title		Eaglelake (10 of 10)
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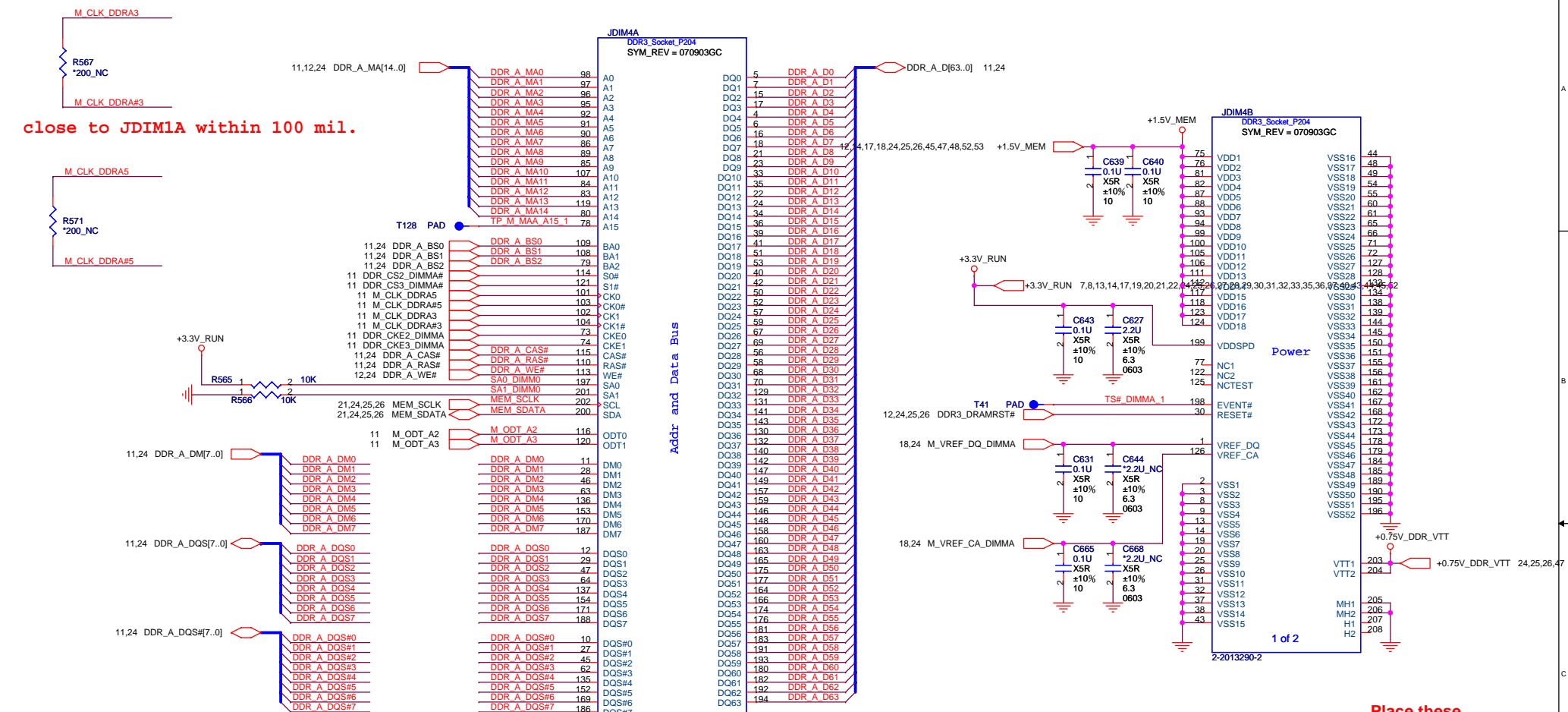






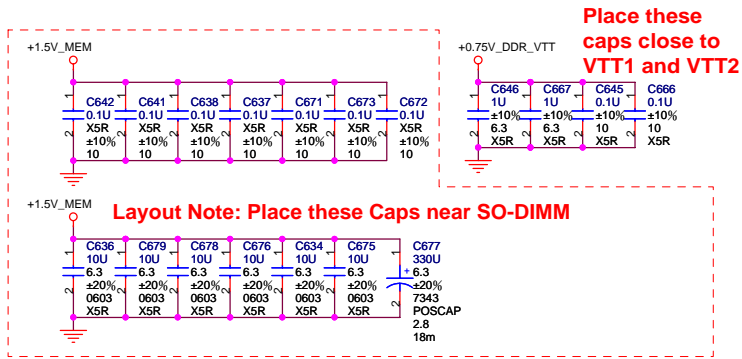







Select the Serial Presence Detect and Temp sensor base address.

	SA1	SA0	Note
CHA0	0	0	
CHA1	0	1	Pull-High to +3.3V_RUN
CHB0	1	0	
CHB1	1	1	

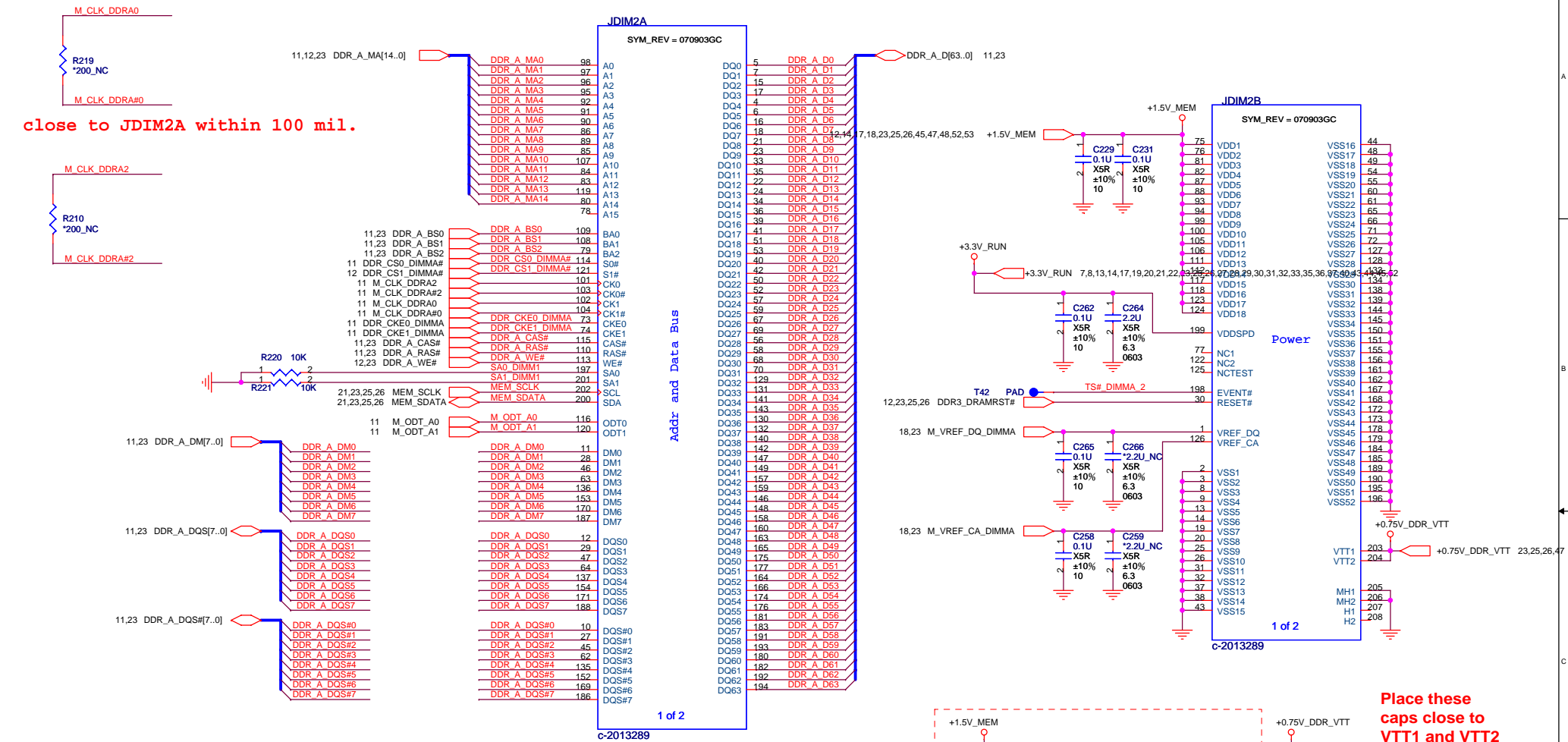




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Project Name: **Nike**

Title DDR3 Channel A0 (1 of 5)		
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CHA\_DIMM0\_TOP Layer




Select the Serial Presence Detect and Temp sensor base address.

	SA1	SA0	Note
CHA0	0	0	
CHA1	0	1	Pull-High to +3.3V_RUN
CHB0	1	0	
CHB1	1	1	

Place these caps close to VTT1 and VTT2

Layout Note: Place these Caps near SO-DIMM



**Quanta Computer Inc.**  
Project Name: Nike

Title DDR3 Channel A1 (2 of 5)		
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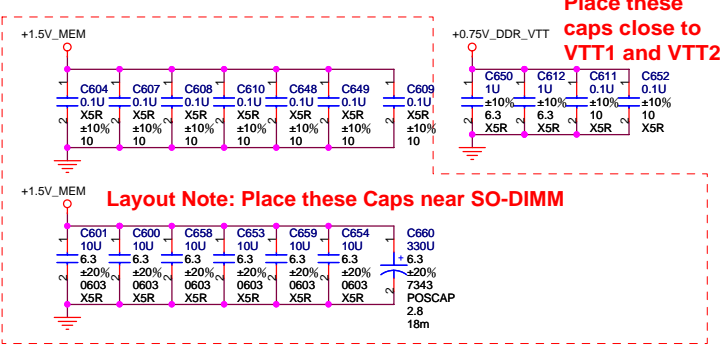
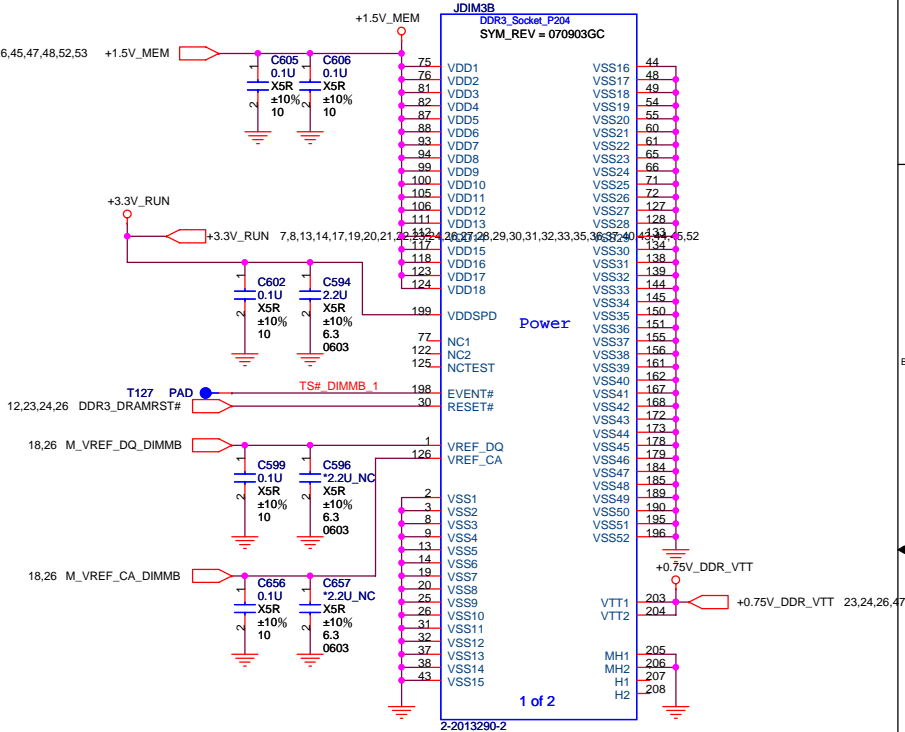
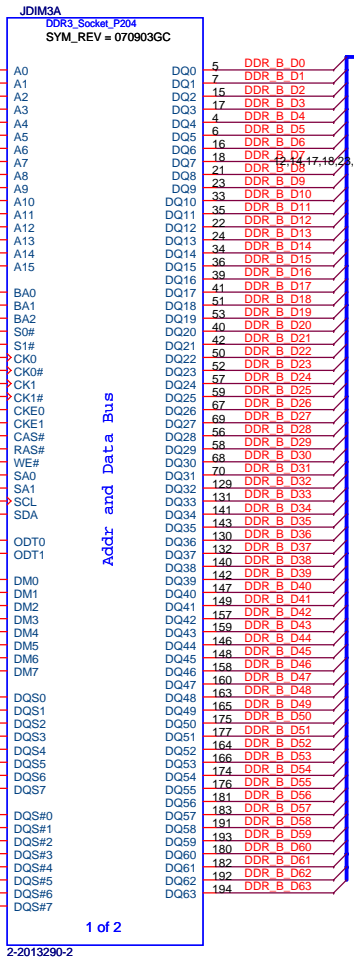



close to JDIM4A within 100 mil.

close to JDIM4A within 100 mil.

Select the Serial Presence Detect and Temp sensor base address.

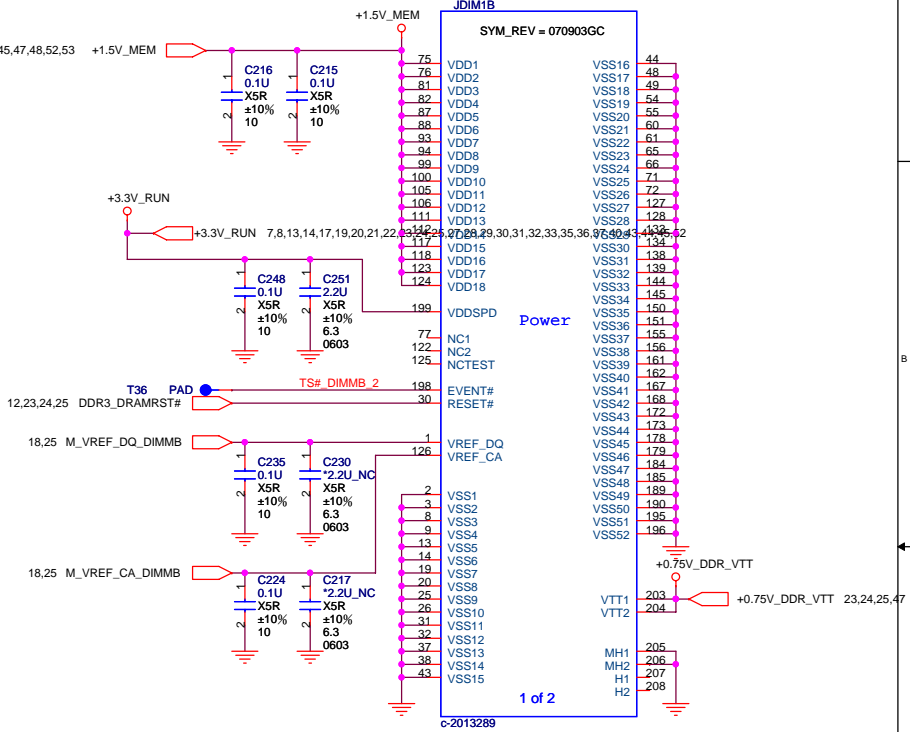
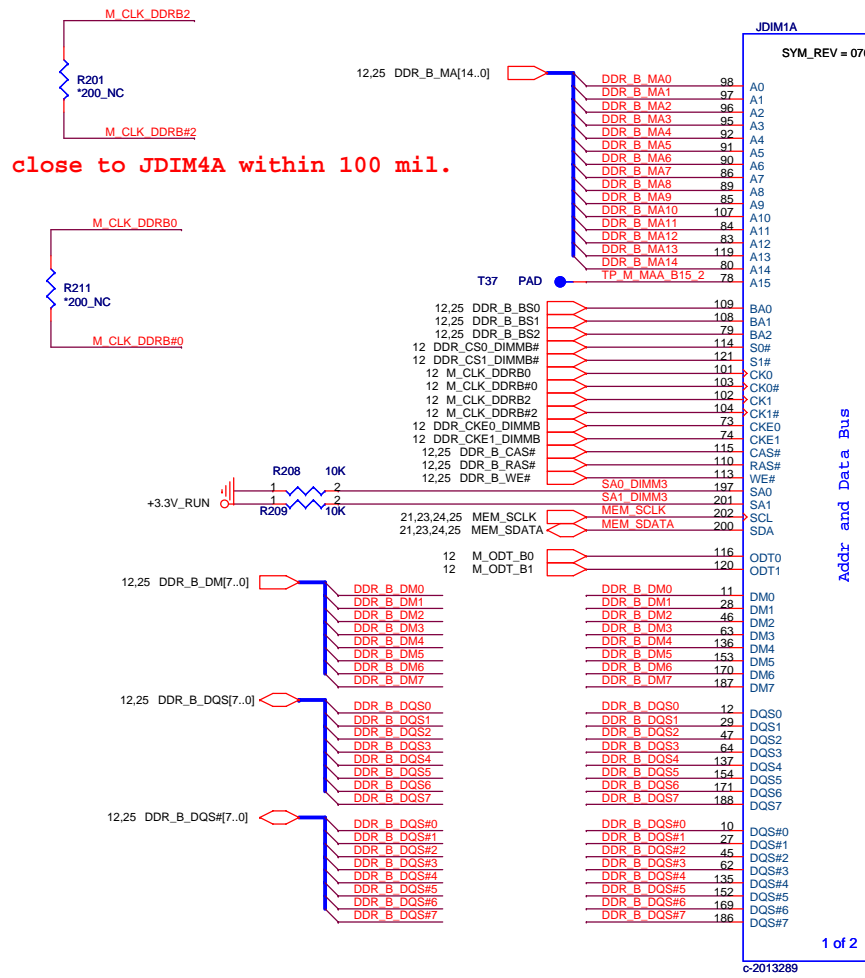
	SA1	SA0	Note
CHA0	0	0	
CHA1	0	1	Pull-High to +3.3V_RUN
CHB0	1	0	
CHB1	1	1	





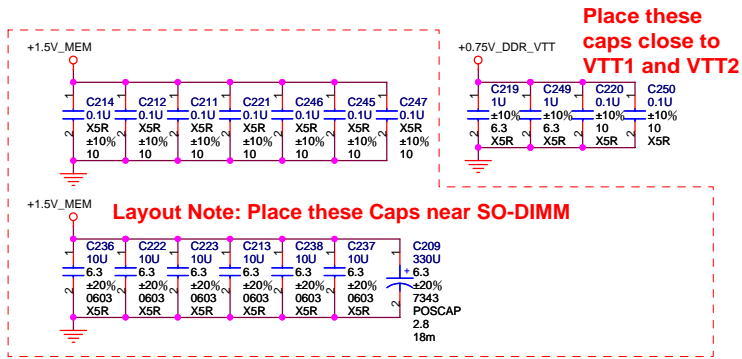
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Project Name: Nike


Title DDR3 Channel A0 (3 of 5)		
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Select the Serial Presence Detect and Temp sensor base address.

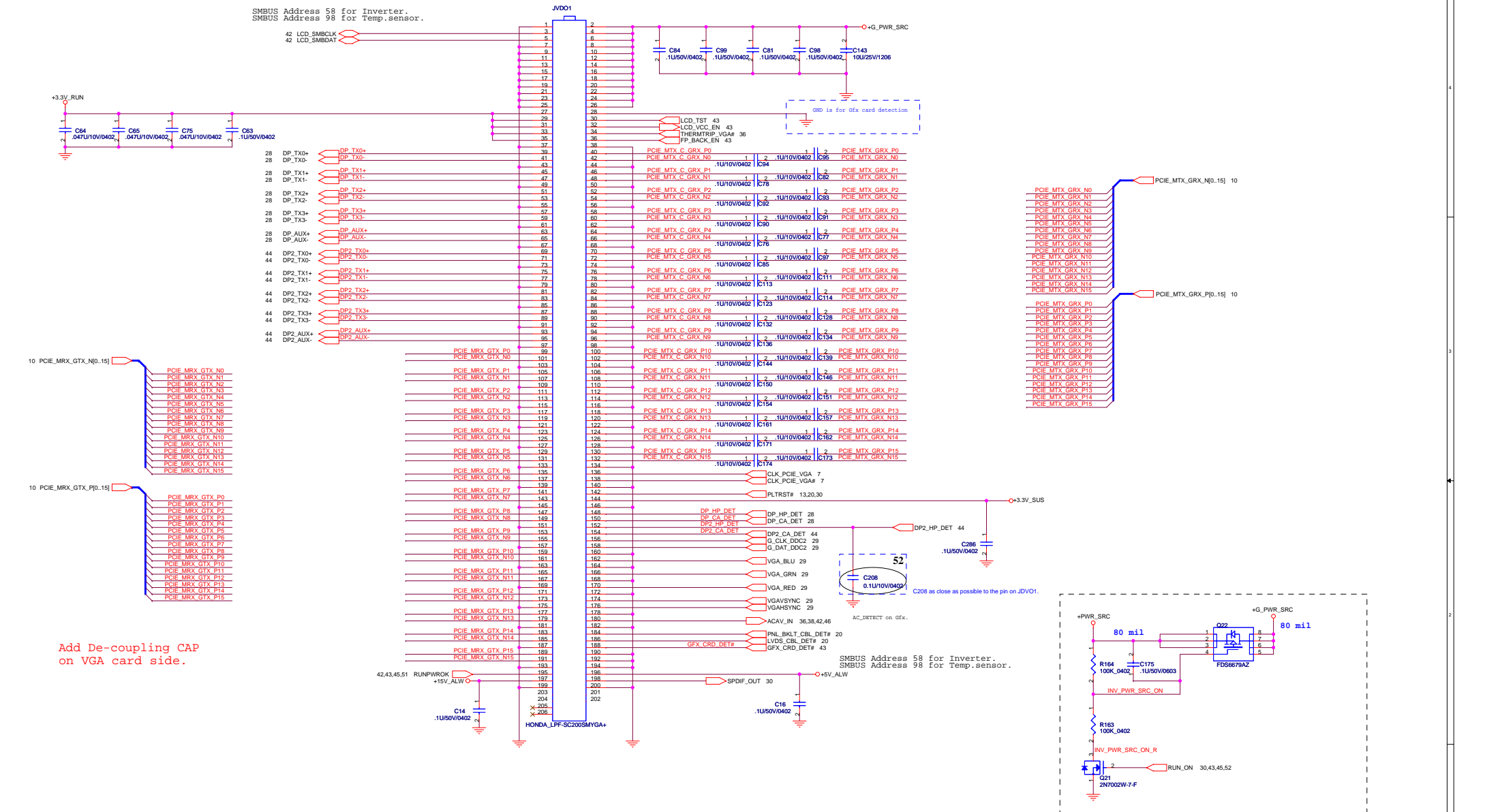
	SA1	SA0	Note
CHA0	0	0	
CHA1	0	1	Pull-High to +3.3V_RUN
CHB0	1	0	
CHB1	1	1	



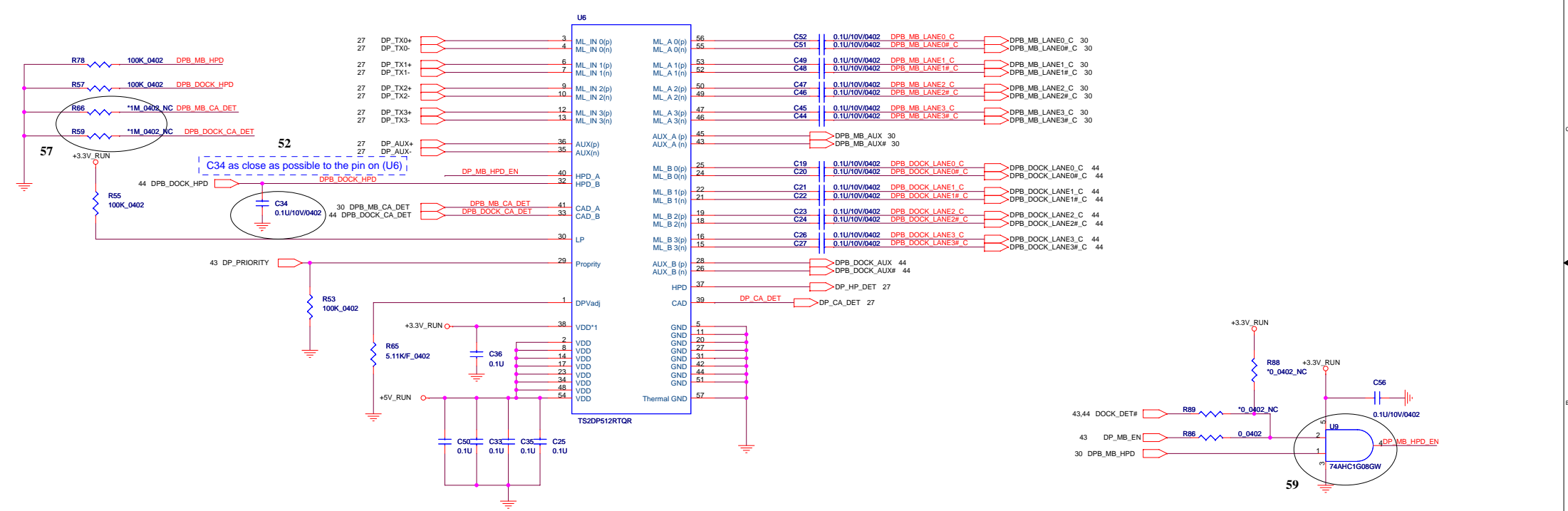


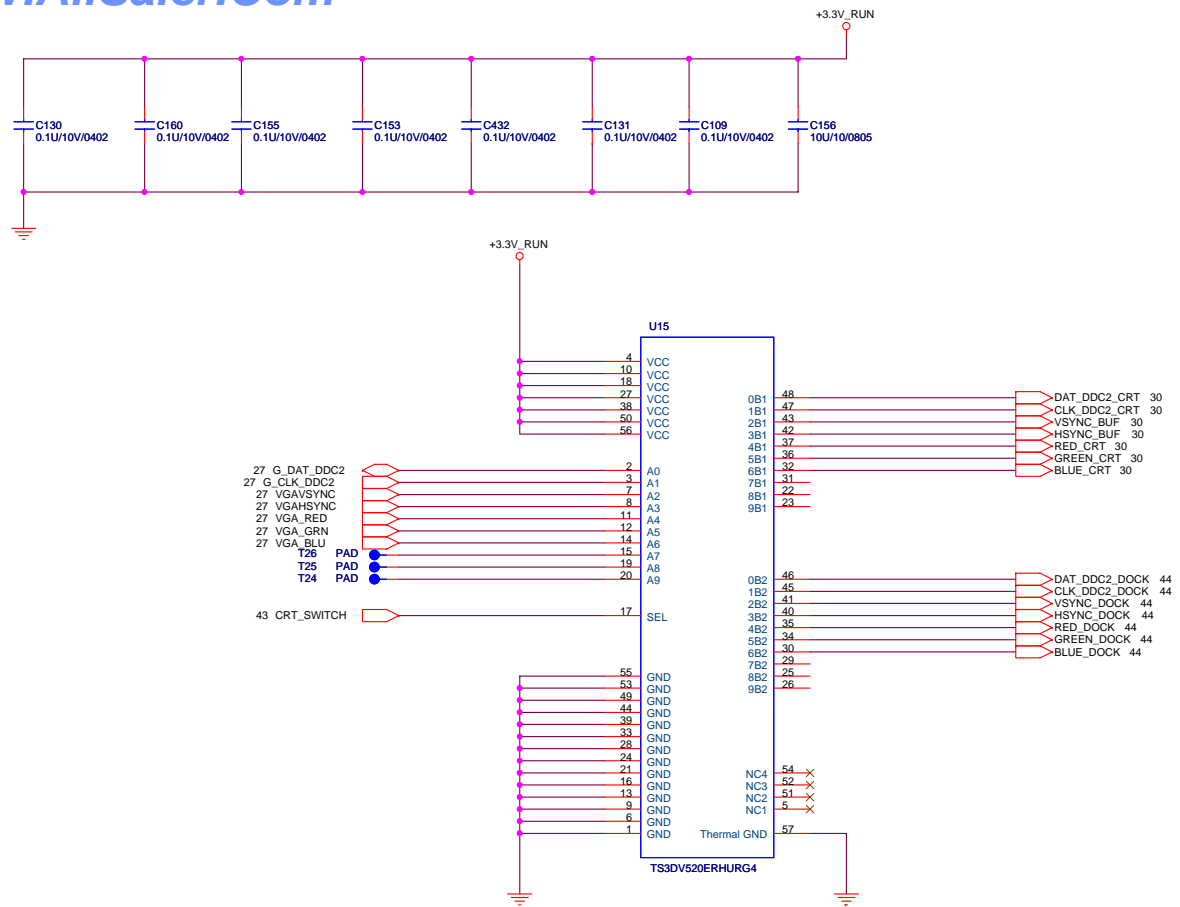
**Quanta Computer Inc.**  
Project Name: **Nike**

Title DDR3 Channel A0 (4 of 5)		
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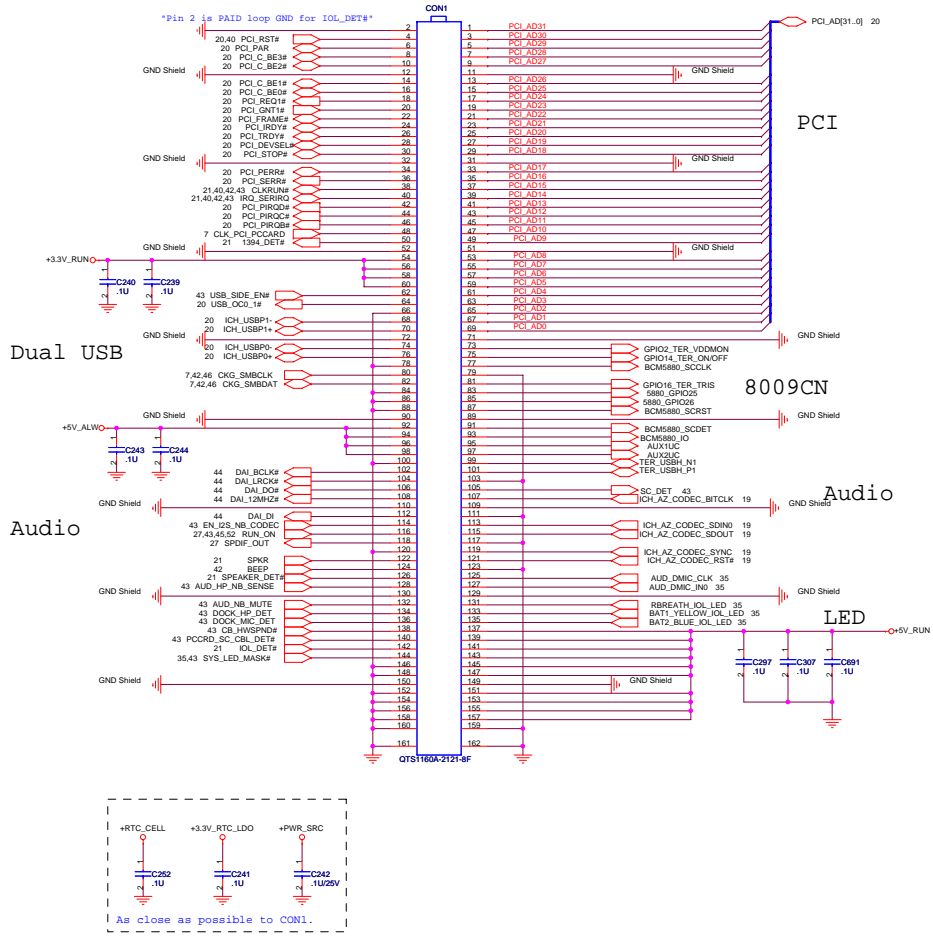


Add De-coupling CAP  
on VGA card side.

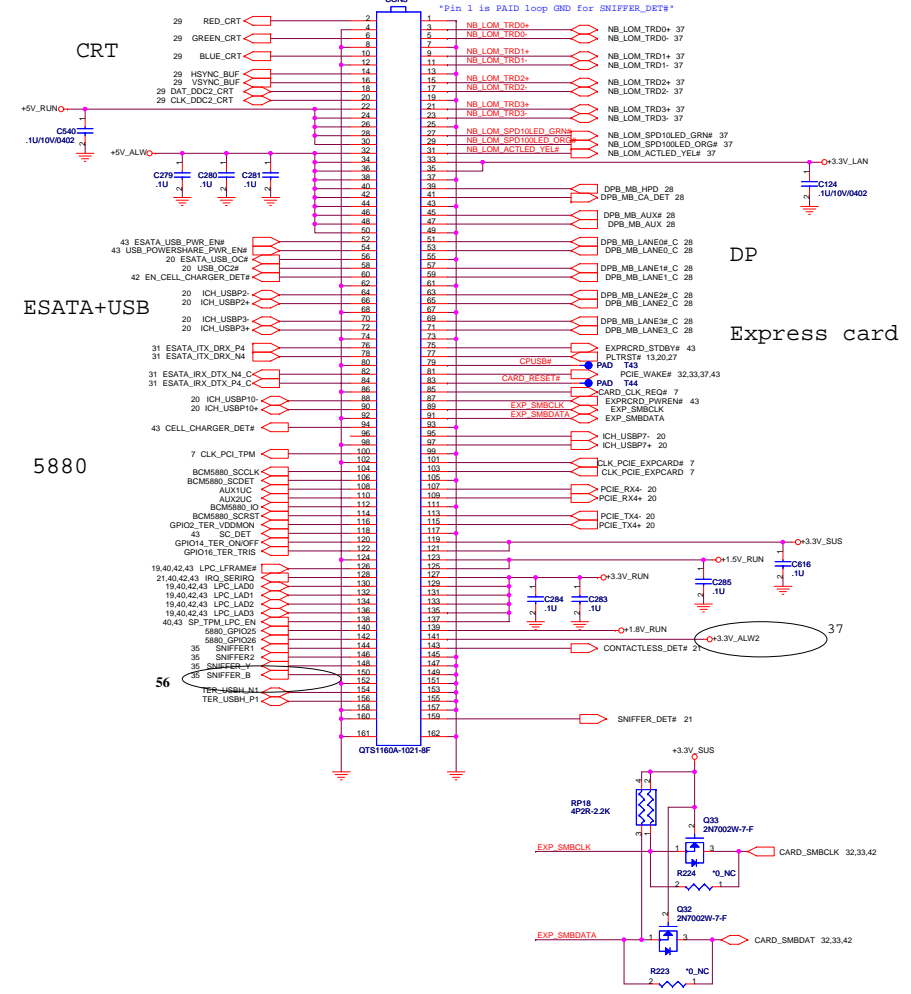


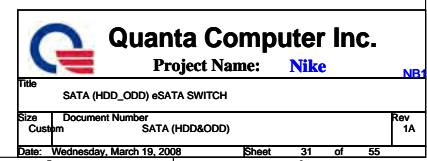


IOL CONNECTER



IOR CONNECTER

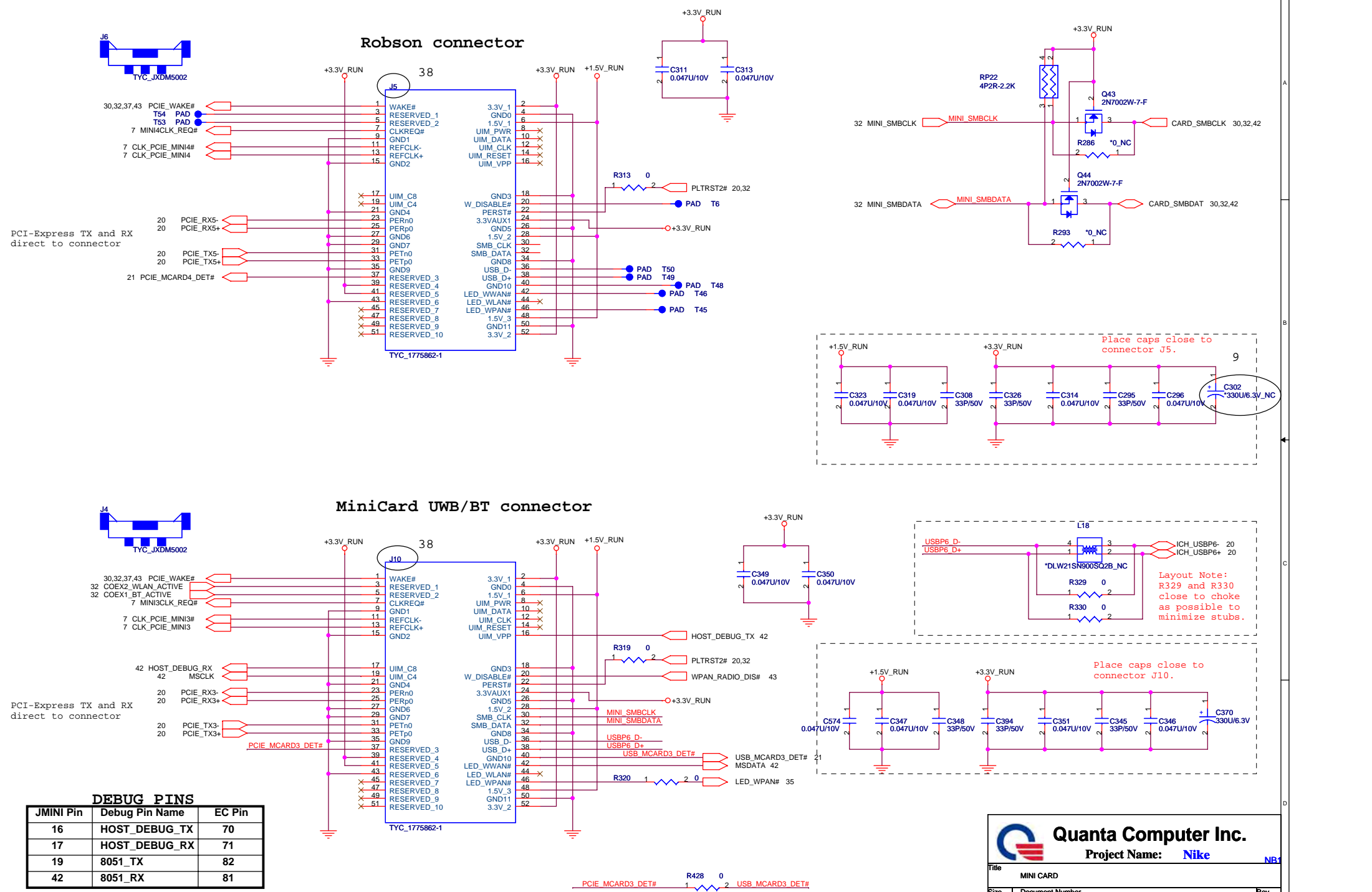













PCI-Express TX and RX direct to connector

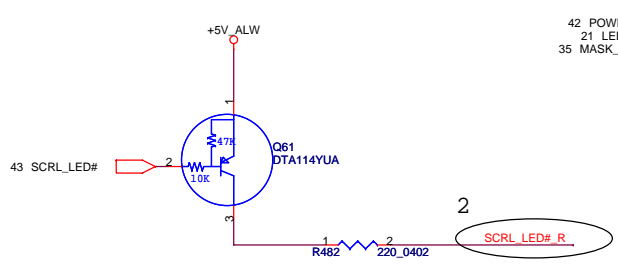
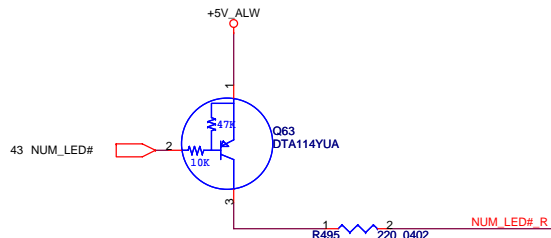
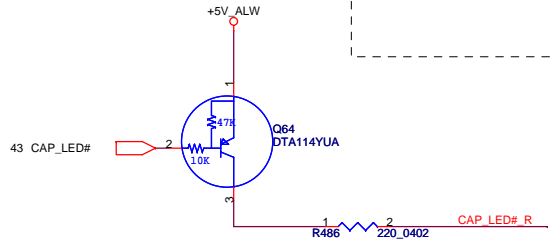
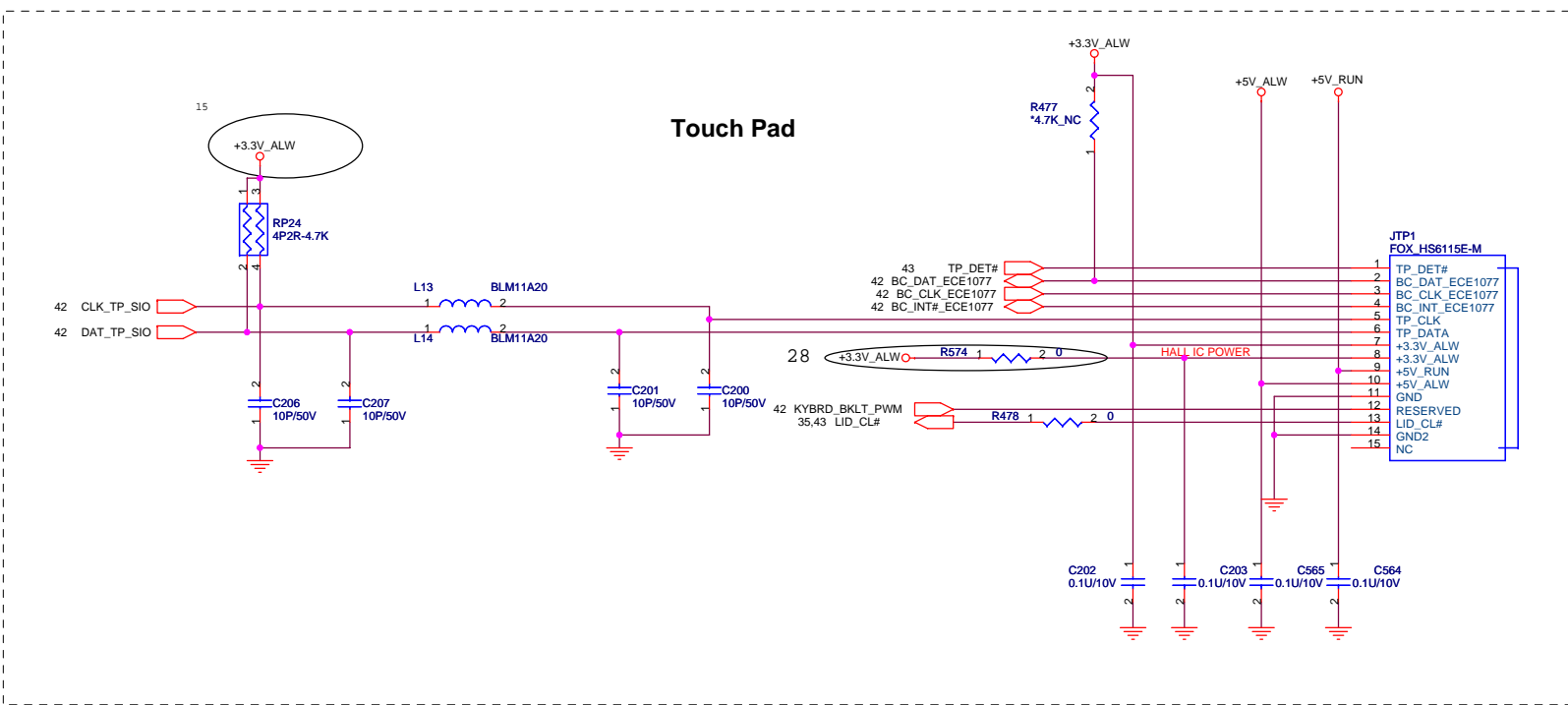
PCI-Express TX and RX direct to connector



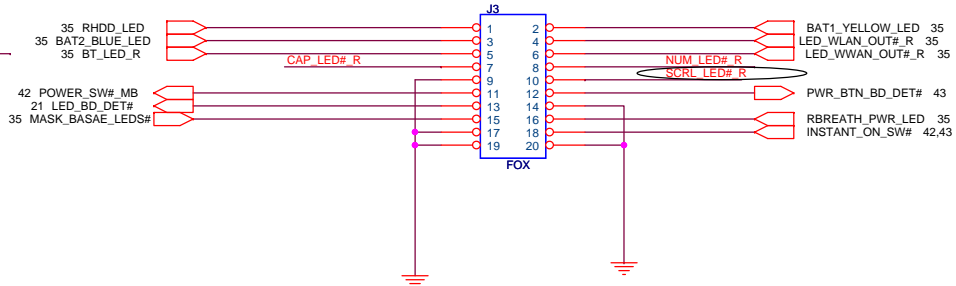
**Quanta Computer Inc.**  
Project Name: **Nike**

Title MINI CARD		
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DEBUG PINS		
JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



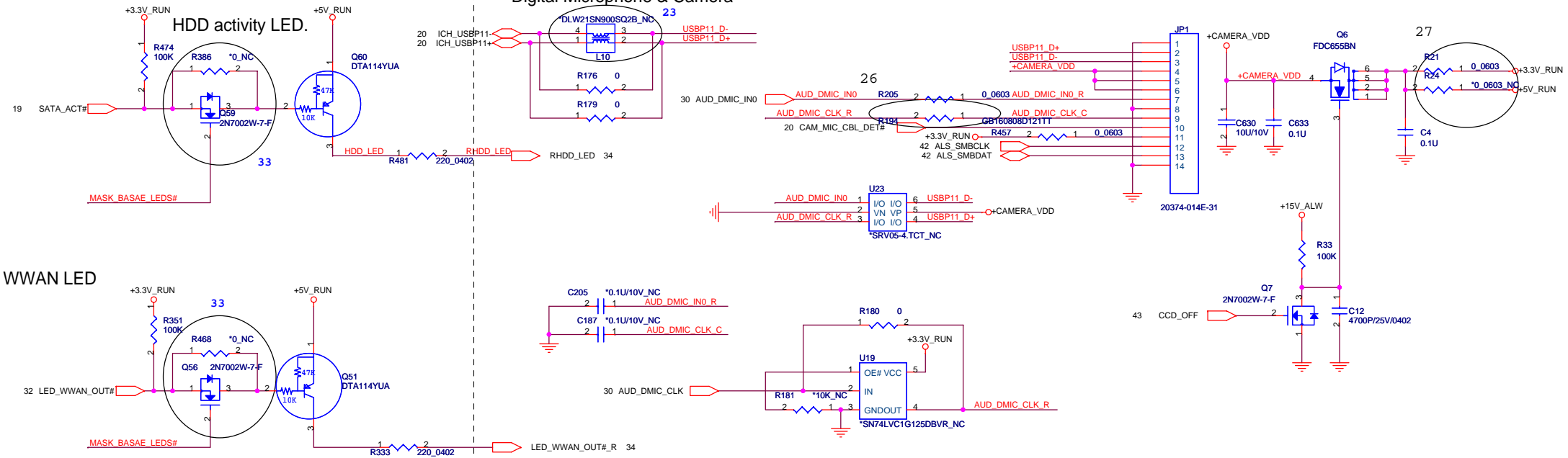
PWR\_BTN board connector



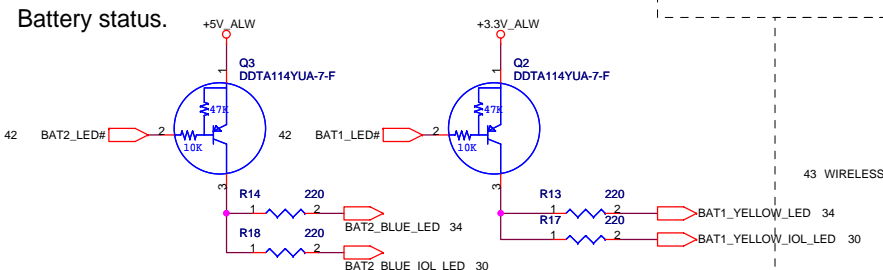
**Quanta Computer Inc.**  
Project Name: **Nike**

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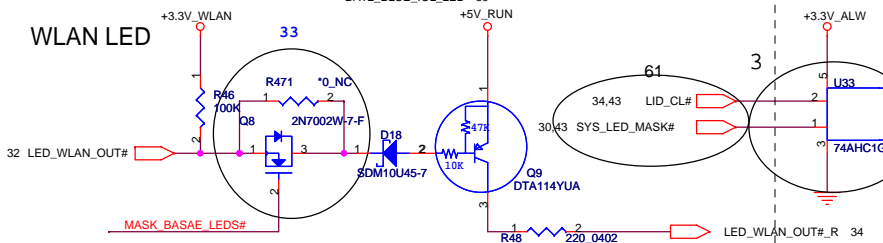
### Digital Microphone & Camera



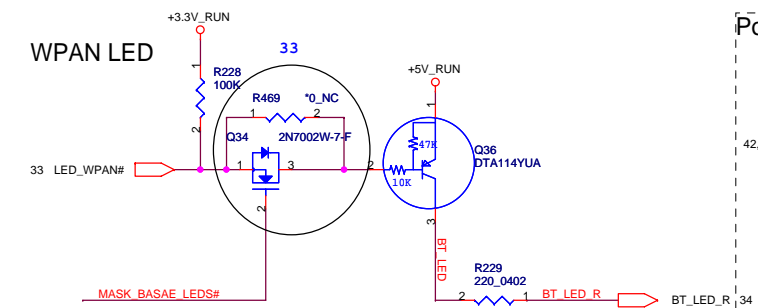
Battery status.



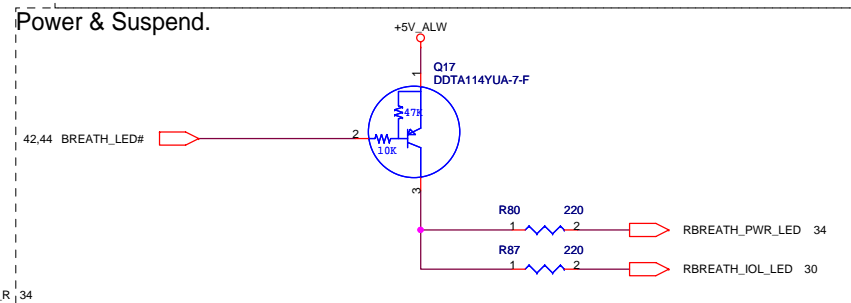
## WLAN LED



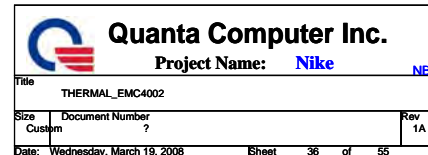
## WPAN LED

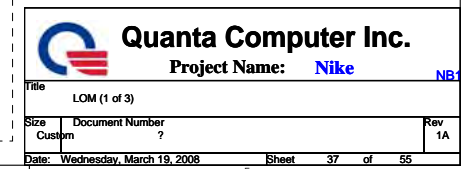
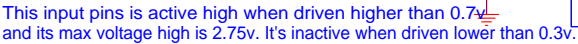


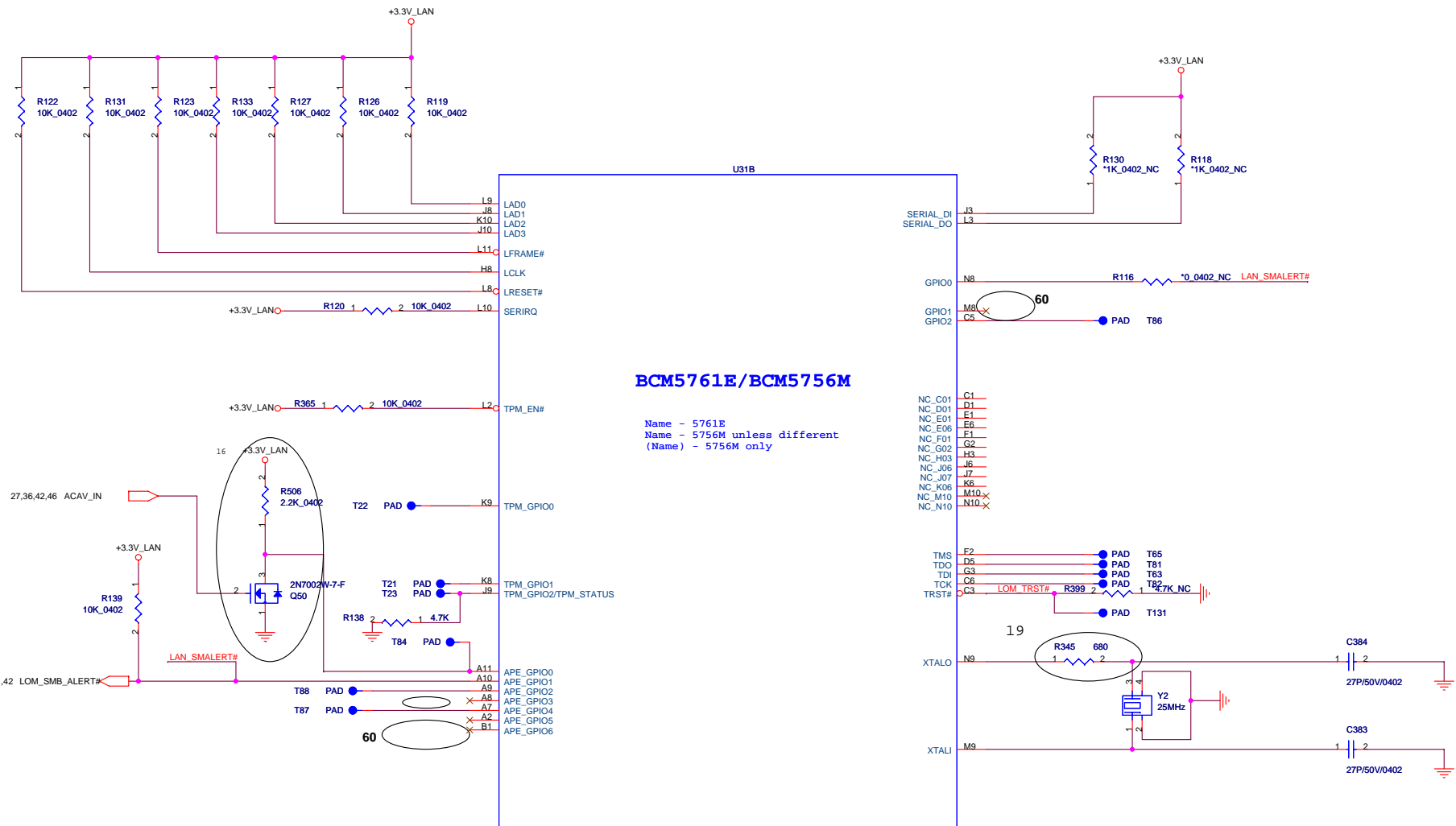
## Power &amp; Suspend.



	SYS_LED _MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base LEDs (Lid Closed)	1	0
Do Not Mask LEDs (Lid Open)	1	1








BCM5761E/BCM5756M

Name - 5761E  
Name - 5756M unless different  
(Name) - 5756M only

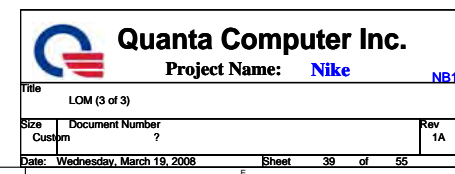


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Project Name: Nike

NB3

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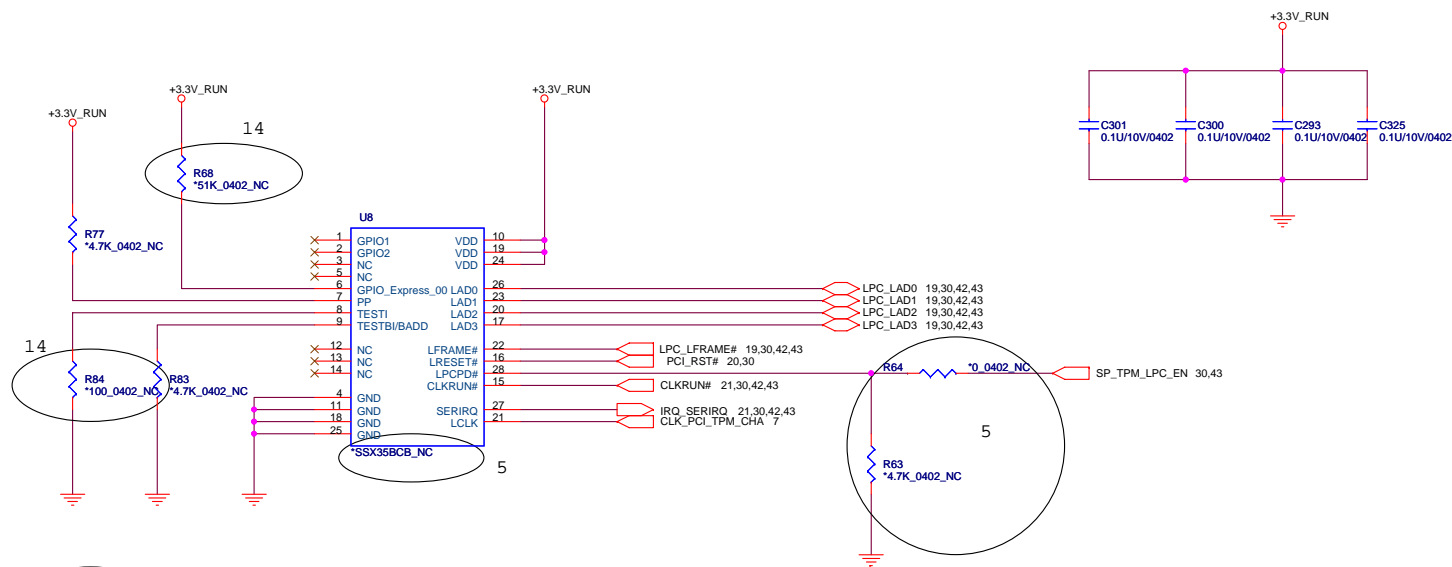
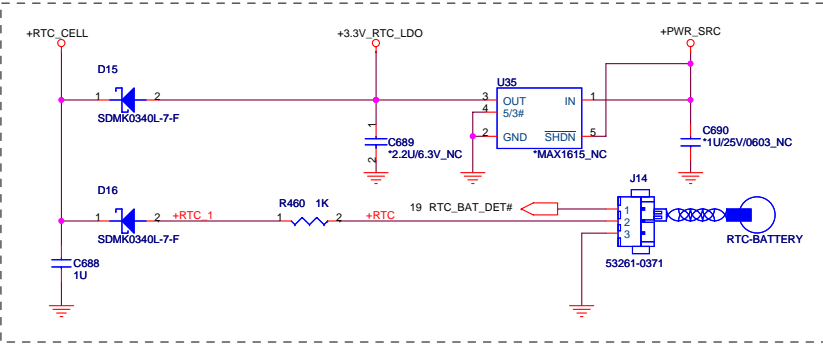


Table1

BOM option scheme for USH TPM vs China TPM				
		B0 USH		No TPM
MB	MB,U8	NC		NC
	MB,R27	NC		NC
	MB,R63	NC		NC
	MB,R64	NC		NC
	R77,R68,R84,R83	NC		NC
	MB,R149	POP		POP
	MB,R151	NC		NC
	MB,R156	NC		NC
	MB,R434	POP		POP

RTC BATTERY



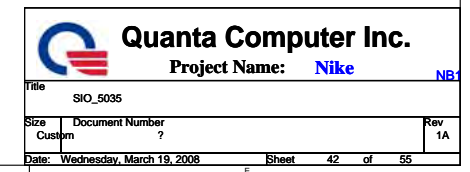
Quanta Computer Inc.

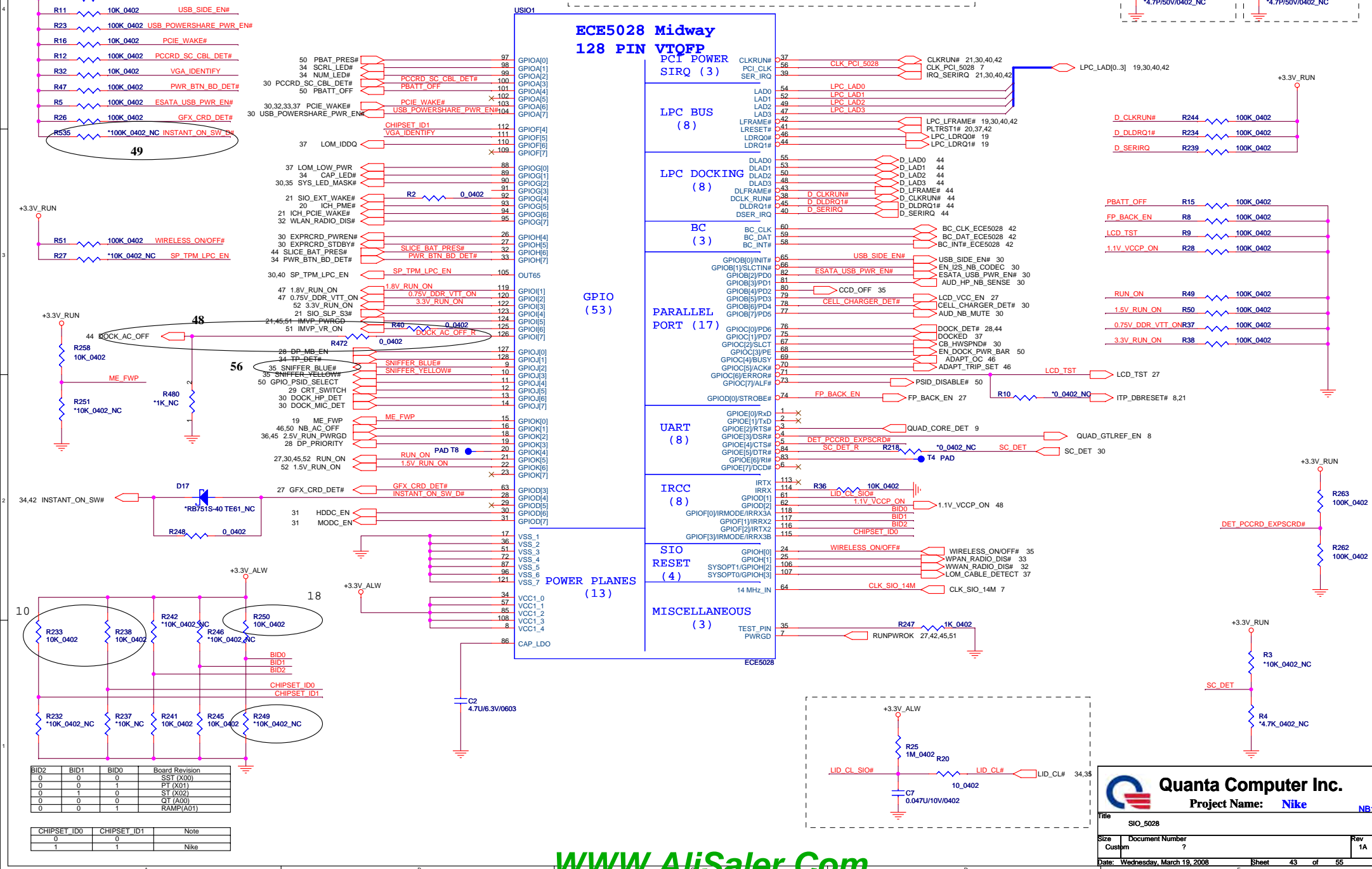
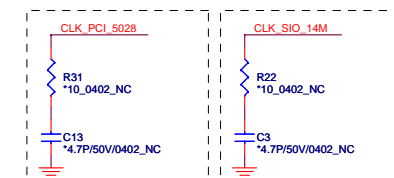
Project Name: Nike NB3

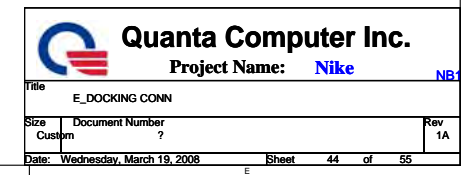
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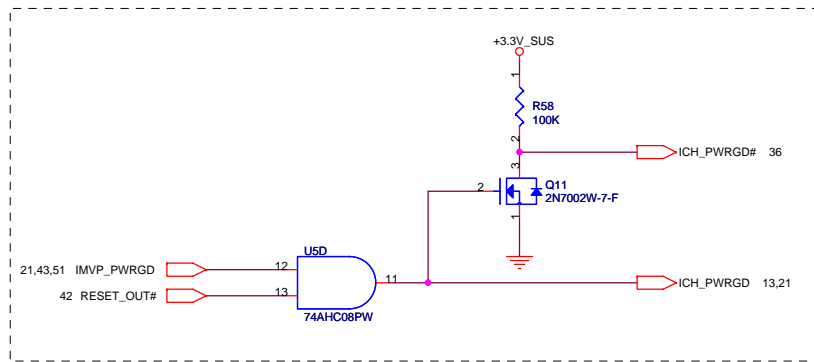
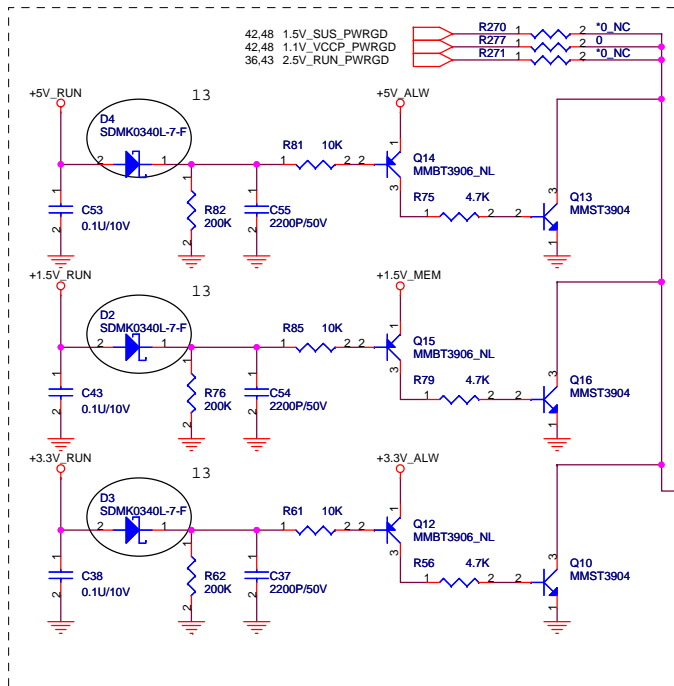
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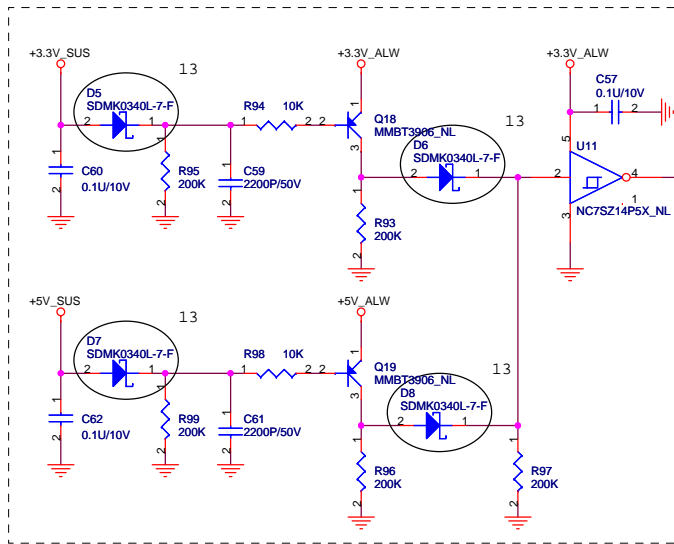
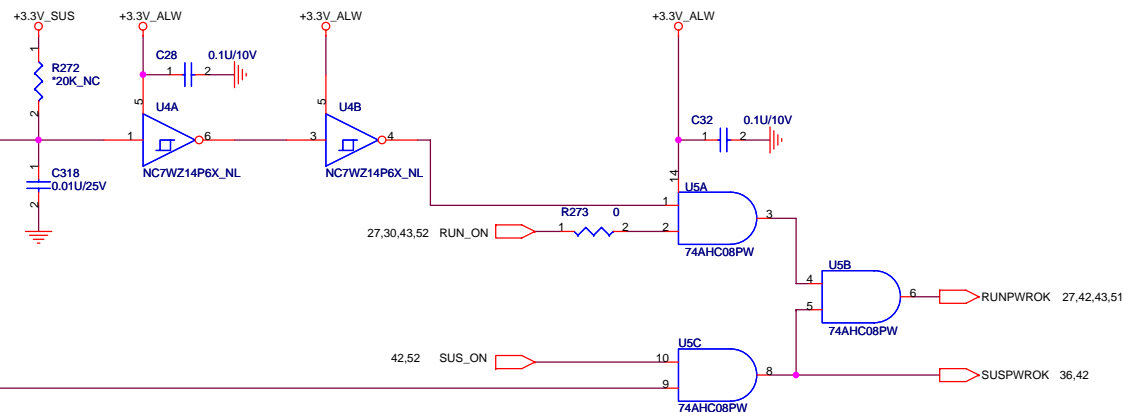








Keep Away from high speed buses

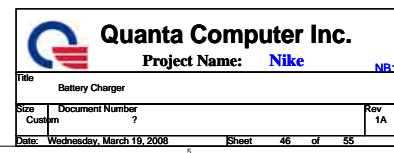


**Quanta Computer Inc.**  
Project Name: **Nike**

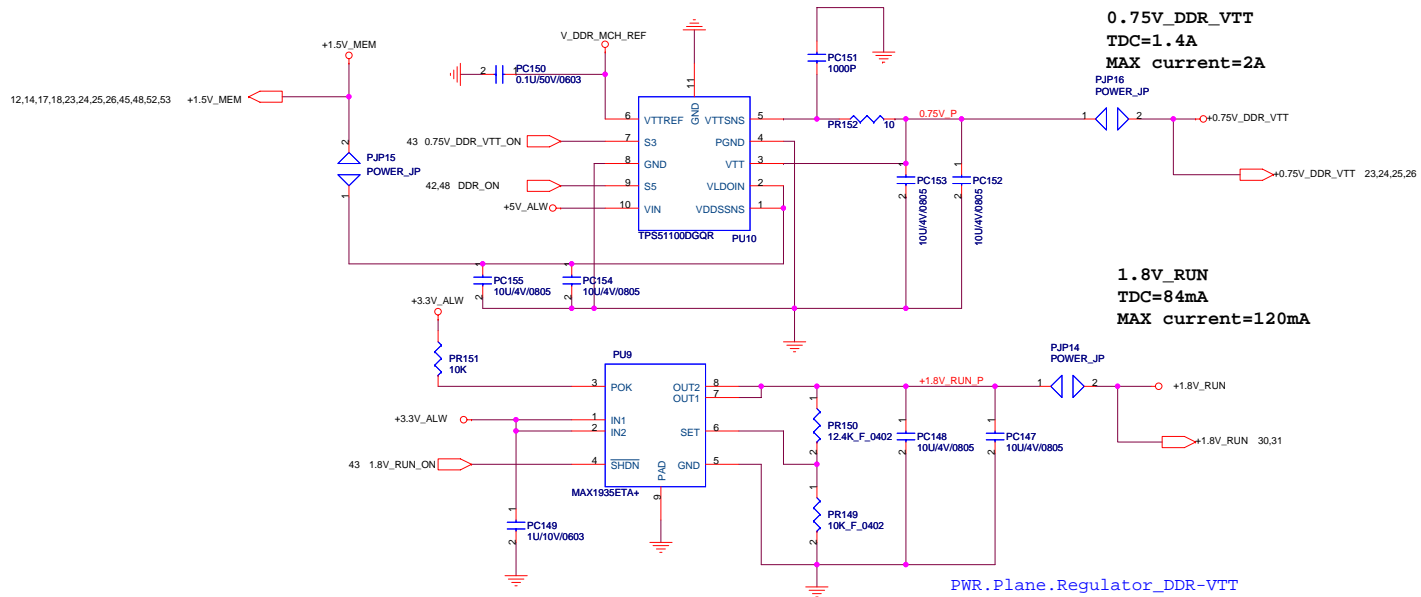
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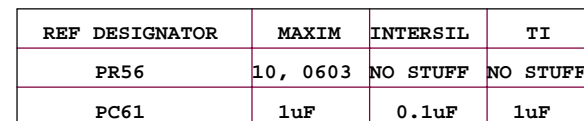
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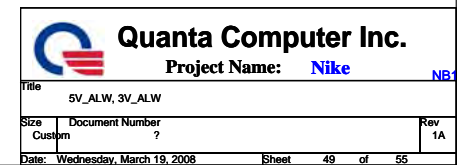
Date: Wednesday, March 19, 2008 Sheet 45 of 55

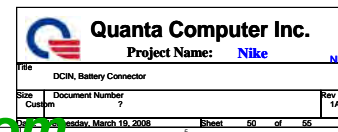


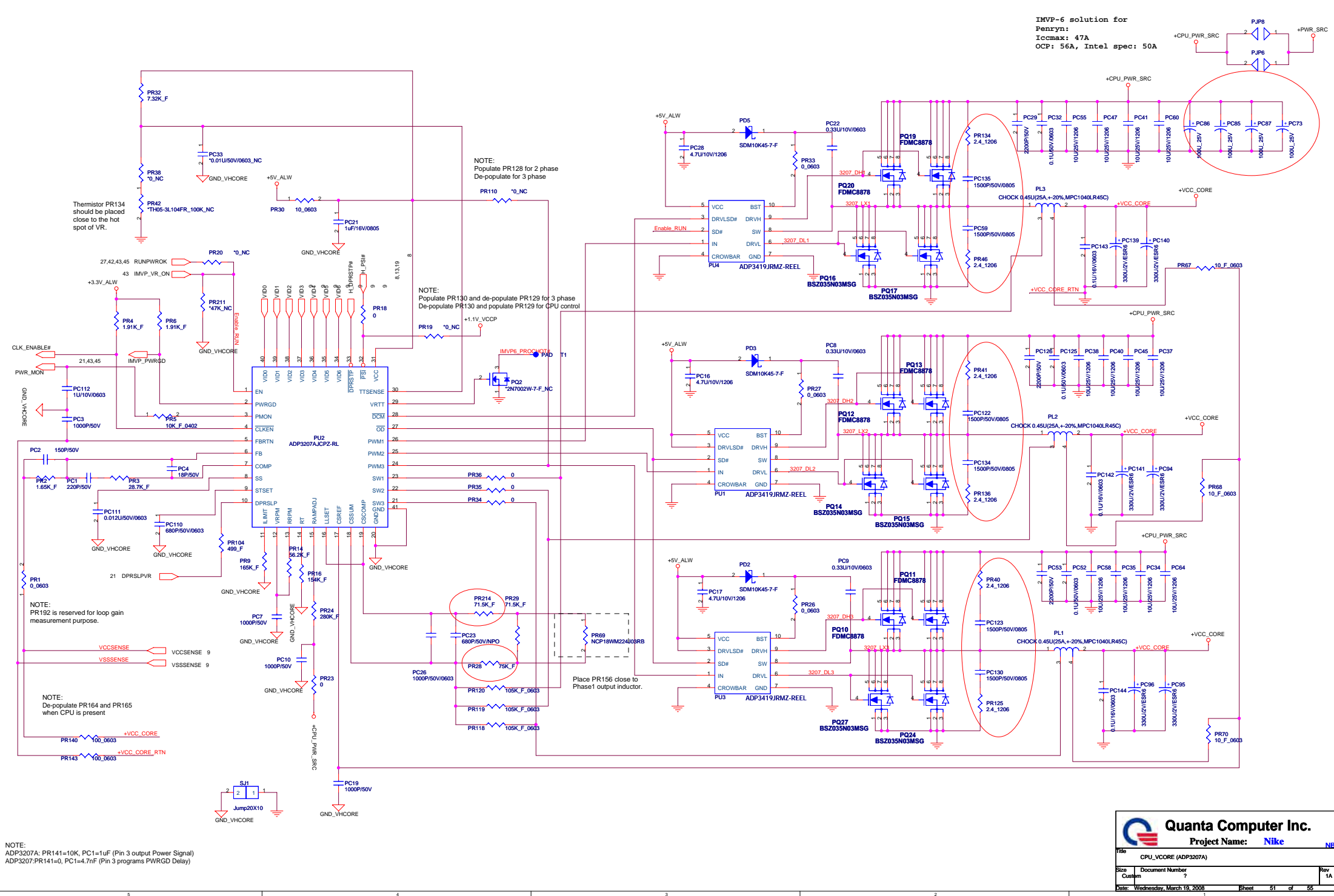


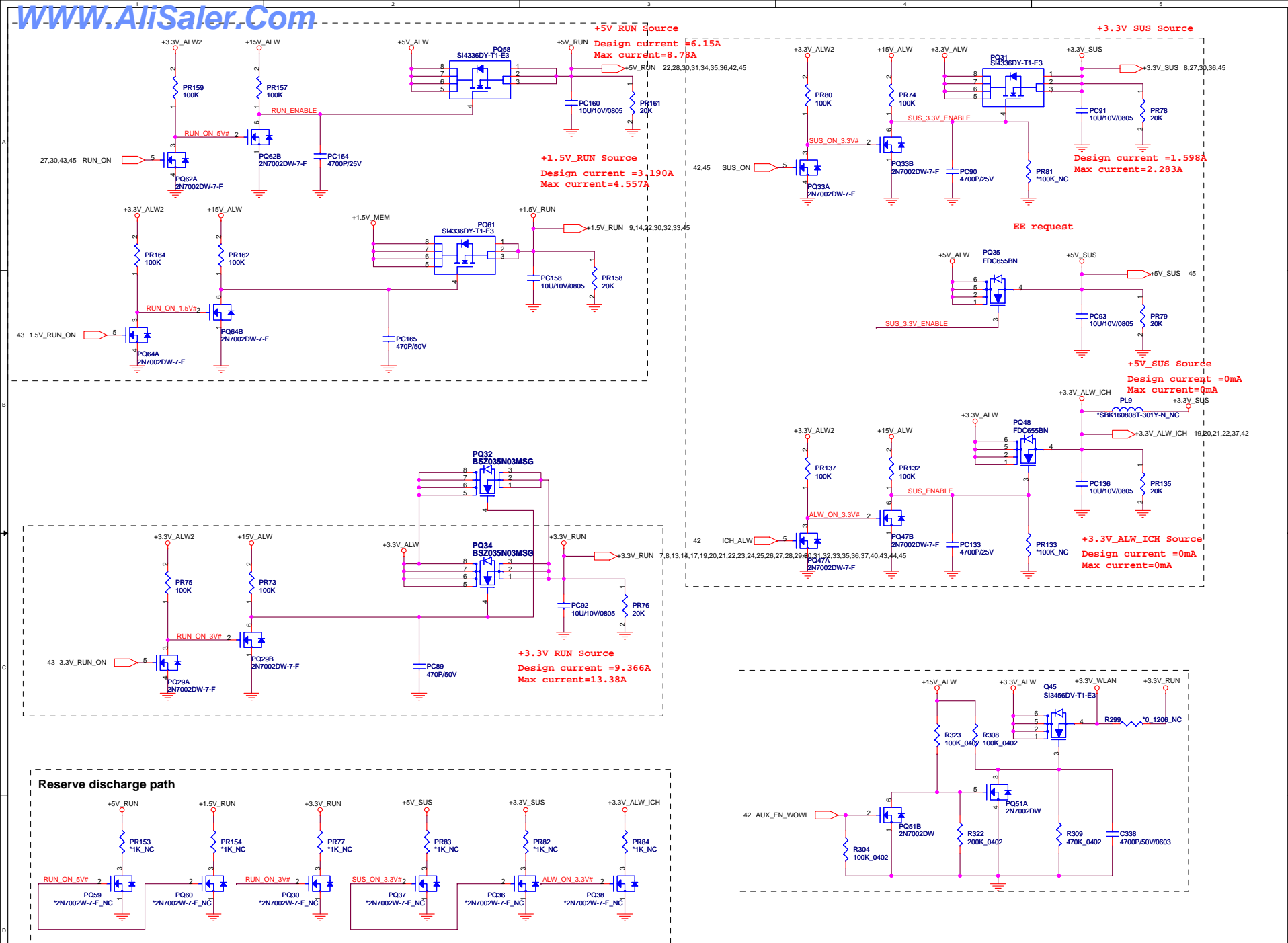


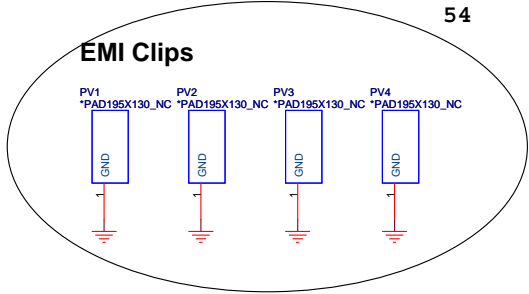
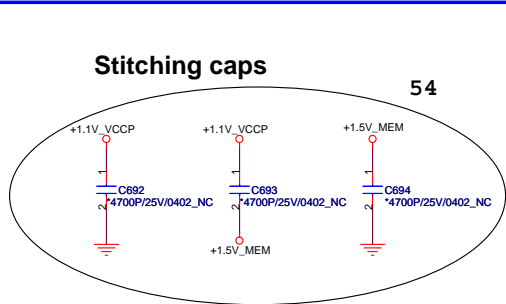
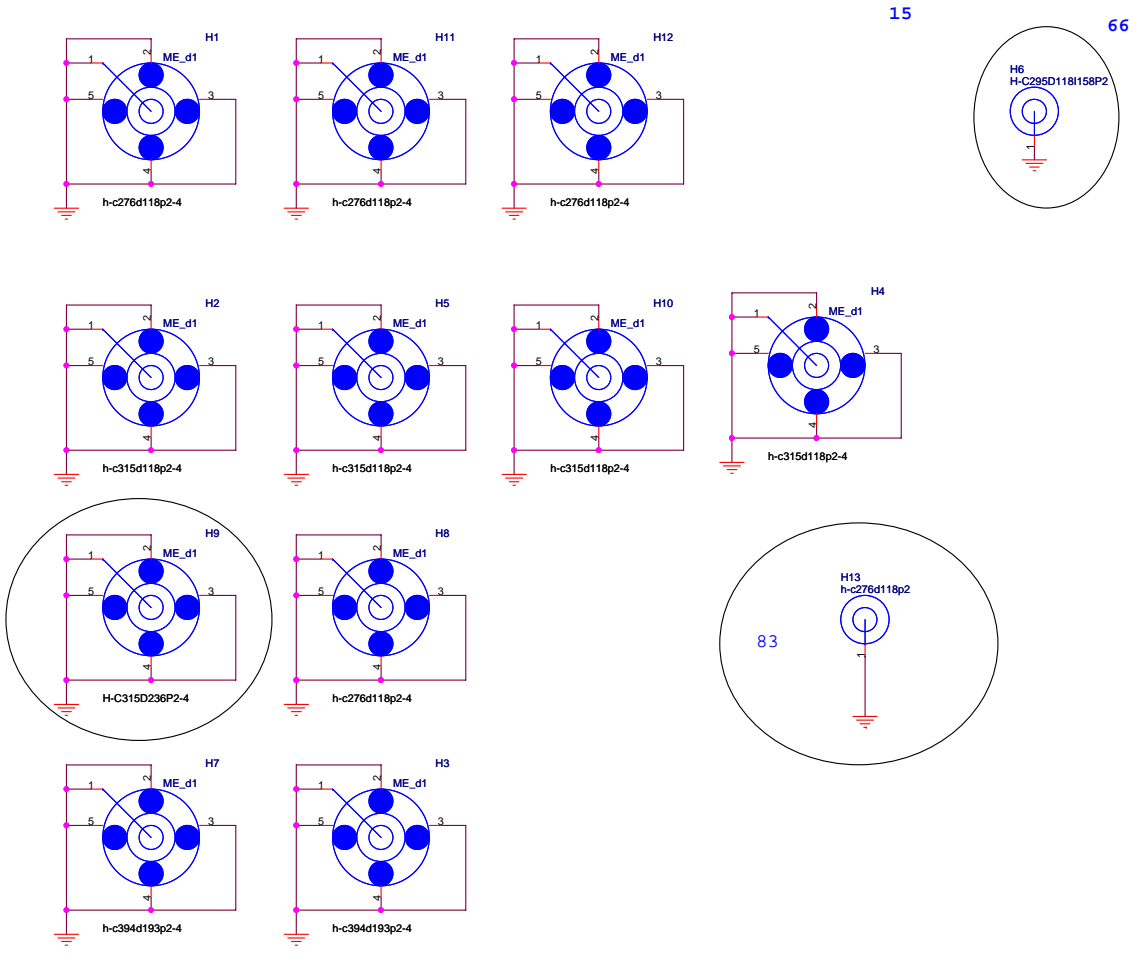

















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Model	Item	Page	Date	Rev.	Description
XM1 MB	38	32,33	0313	X01	MPCI socket needs to change source priority from Molex to Tyco. Molex has quality issue of solder tails coplanarity and that will impact to SMT performance.
	39	42	0314	X01	Depop J9 and J13 debug connectors from M/B.
	40	36	0314	X01	Remove U34 pin 50~57 for layout symbol change.
	41	19,31	0314	X01	Change C470~C473, C466~C469, C663~C664, C682,C683,C255 and C256 from 3900pf to 0.01uf per Intel schematics.
	42	36, 8	0314	X01	Del C617, R472, R480. Add Q68, C695 for New thermal sensor locations from thermal team.
	43	32	0315	X01	Populate R240 on WIMAX_LED signal for WiMAX LED support & test.
	44	21,42	0315	X01	Work Item SCH169422: X01: MB : Change PORT_SELECT to MEC GPIO per BIOS request
	45	35	0315	X01	Work Item SCH169263: X01: MB: No-pop duplicate pull-up on Sniffer_Pwr_Sw# and Wireless_On/Off#
	47	36	0315	X01	Work Item SCH169379: X01: MB : Add a 10K pull-down option on LDO_SHDN# (EMC4002)
	48	43	0315	X01	SCH169440: X01: MB : Add pull-down option on DOCK_AC_OFF
	49	43	0315	X01	SCH169374: X01: MB : Instant_On_Sw# has duplicate pull-up's to +3.3V_ALW
	50	43	0315	X01	SCH169439: X01 : MB : Change ALS SMBus circuit
	51	46	0315	X01	X01: MB : Power circuit changes
	52	28,44	0315	X01	SCH169313: EMI - Aligning w/Roush for DP Enhanced ESD Issue
	53	8	0315	X01	SCH169312: Aligning w/Roush on Enhanced ESD Issues w/E-Dock
	54	9	0315	X01	SCH169254: Changes for QC CPU support
	55	9	0315	X01	EEFCX0D271R (CH727RM8810) to replace EEFUE0D271R (CH7270LM885 => EOL)
	56	35,43	0315	X01	SCH169326: X01: MB, IOR: Change to the Sniffer LED net name & power rails.
	57	8,9	0318	X01	Update CPU socket PN from DGG^9000001 to DGG^9000002.
	58	51	0318	X01	PC85~PC87, PC73 change to stuff.
	59		0318	X01	U9,U25,U33,U24 need change to AL1G0008039
	60	37~39	0319	X01	Del test pad T56, T62, T69, T75, T80, T83 per DFx request for LOM chip.
	61	35,42	0319	X01	Swap pin 1& pin 2 net for AND gate logic change to "H" type (Not HC)
<div>  <div> <div>Quanta Computer Inc.</div> <div>Project Name: ?</div> </div> </div> <div> <div>Title</div> <div>&lt;Title&gt;</div> </div> <div> <div>Size</div> <div>Custom</div> </div> <div> <div>Document Number</div> <div>?</div> </div> <div> <div>Rev</div> <div>?</div> </div> <div> <div>Date:</div> <div>Wednesday, March 19, 2008</div> </div> <div> <div>Sheet</div> <div>55</div> <div>of</div> <div>55</div> </div>					
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